DATA SHEET

SAA7140A; SAA7140B
High Performance Scaler (HPS)

Objective specification
Supersedes data of 1996 Jul 26
File under Integrated Circuits, IC22

1996 Sep 04

Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Scaling of video pictures down to randomly sized windows
- Horizontal upscaling (zoom)
- Two dimensional phase-correct data processing for improved signal quality of scaled data, especially for compression applications
- Processing of a maximum of 2047 active samples per line (V-processing in bypass) and 2047 active lines per frame
- 16-bit YUV data input port
- Bidirectional expansion port with full duplex functionality (D1) or 16-bit YUV input/output
- Discontinuous data stream supported
- Field-wise switching between two data sources
- Two independent I^2C-bus programming sets
- Brightness, contrast and saturation controls for scaled outputs
- Chroma key (α generation)
- YUV-to-RGB conversion including anti-gamma correction for RGB
- 16-word FIFO register for 32-bit output data
- Output configurable for 32, 24, 16 and 8-bit video data
- Scaled 16-bit 4 : 2 : 2 YUV output
- Scaled 15-bit RGB (5, 5, 5) + α with dither and 24-bit RGB (8, 8, 8) + α output
- Scaled 8-bit monochrome output
- Four independent user configurable general purpose I/O pins
- Low power consumption in I^2C-bus controlled pseudo sleep mode
- **Support of 5 V (SAA7140A) and pure 3.3 V (SAA7140B) signalling environment**.

2 GENERAL DESCRIPTION

The SAA7140A and SAA7140B are CMOS High Performance Scaler (HPS) and is a highly integrated circuit designed for use in DeskTop Video (DTV) applications. The devices resample digital video signals using two dimensional phase-correct interpolation in order to display it in an arbitrarily sized window.

The SAA7140A fits perfectly into a 5 V signal environment and requires two different supply voltages (5 V and 3.3 V). The SAA7140B is a pure 3.3 V design and therefore has only 3.3 V supply pins. With respect to functions and programming, both devices are identical.

The devices incorporate additional functions such as control of brightness, saturation, contrast, chroma key generation, YUV-to-RGB conversion, compensation of gamma precorrection, dithering and choice of several output formats.

The SAA7140A and SAA7140B accepts data from 1 or 2 input signal sources, via it's 16-bit YUV input port and/or the bidirectional expansion port. They deliver scaled data on the 32-bit VRO output port and, if selected, also on the bidirectional expansion port. A synchronous (transparent) together with an asynchronous (burst) data transfer mode is supported at the 32-bit VRO port.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7140A	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1
SAA7140B	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

4 BLOCK DIAGRAMS

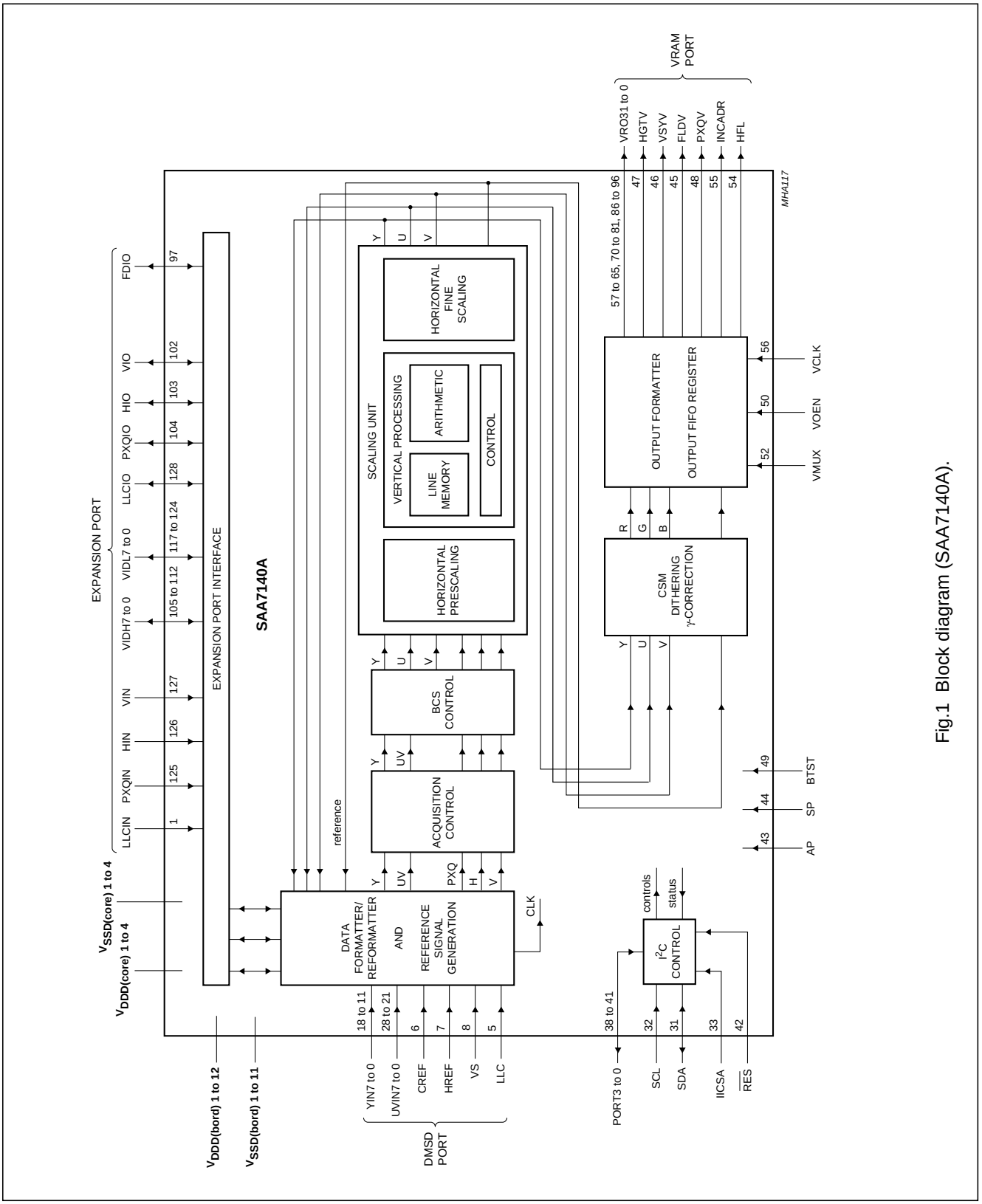


Fig.1 Block diagram (SAA7140A).

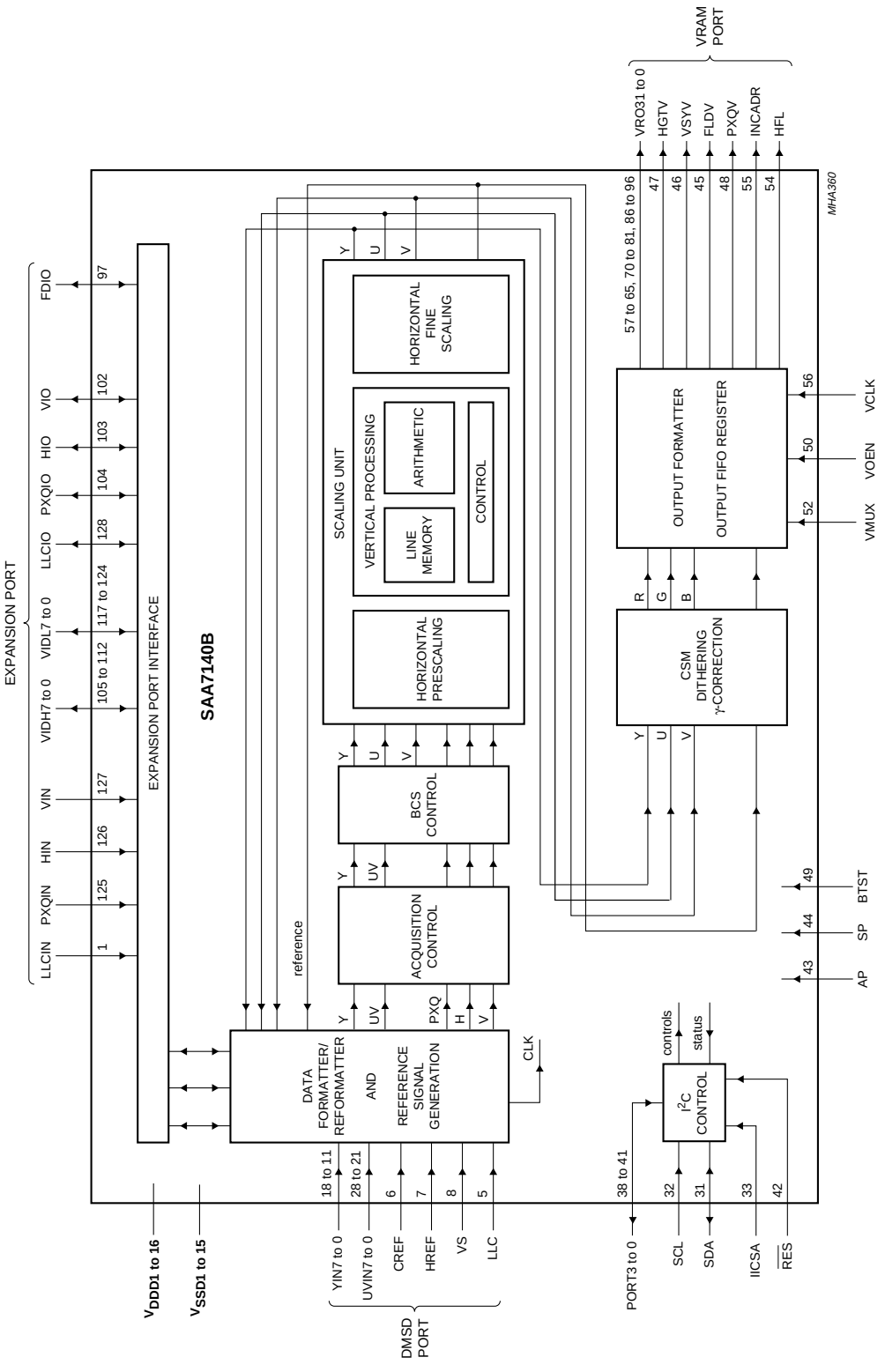


Fig.2 Block diagram (SAA7140B).

5 PINNING (SAA7140A)

SYMBOL	PIN	I/O	DESCRIPTION
LLCIN	1	I	line-locked system clock input; expansion port
$V_{DDD(bord)1}$	2	–	digital border supply voltage 1 (+5 V)
$V_{SSD(bord)1}$	3	–	digital border ground 1 (0 V)
$V_{DDD(bord)2}$	4	–	digital border supply voltage 2 (+5 V)
LLC	5	I	line-locked system clock input, maximum 32 MHz (2 × pixel rate); DMSD port
CREF	6	I	clock qualifier input (HIGH indicates valid input data YUV on DMSD port)
HREF	7	I	horizontal reference input signal; DMSD port
VS	8	I	vertical sync input signal; DMSD port
$V_{DDD(core)1}$	9	–	digital core supply voltage 1 (+3.3 V)
$V_{SSD(bord)2}$	10	–	digital border ground 2 (0 V)
YIN0	11	I	luminance input data (bit 0); DMSD port
YIN1	12	I	luminance input data (bit 1); DMSD port
YIN2	13	I	luminance input data (bit 2); DMSD port
YIN3	14	I	luminance input data (bit 3); DMSD port
YIN4	15	I	luminance input data (bit 4); DMSD port
YIN5	16	I	luminance input data (bit 5); DMSD port
YIN6	17	I	luminance input data (bit 6); DMSD port
YIN7	18	I	luminance input data (bit 7); DMSD port
$V_{DDD(bord)3}$	19	–	digital border supply voltage 3 (+5 V)
$V_{SSD(core)1}$	20	–	digital core ground 1 (0 V)
UVIN0	21	I	time-multiplexed colour-difference input data (bit 0); DMSD port
UVIN1	22	I	time-multiplexed colour-difference input data (bit 1); DMSD port
UVIN2	23	I	time-multiplexed colour-difference input data (bit 2); DMSD port
UVIN3	24	I	time-multiplexed colour-difference input data (bit 3); DMSD port
UVIN4	25	I	time-multiplexed colour-difference input data (bit 4); DMSD port
UVIN5	26	I	time-multiplexed colour-difference input data (bit 5); DMSD port
UVIN6	27	I	time-multiplexed colour-difference input data (bit 6); DMSD port
UVIN7	28	I	time-multiplexed colour-difference input data (bit 7); DMSD port
$V_{DDD(bord)4}$	29	–	digital border supply voltage 4 (+5 V)
$V_{SSD(bord)3}$	30	–	digital border ground 3 (0 V)
SDA	31	I/O	serial data input/output (I^2C-bus)
SCL	32	I	serial clock input (I^2C-bus)
IICSA	33	I	set address input (I^2C-bus)
$V_{DDD(bord)5}$	34	–	digital border supply voltage 5 (+5 V)
$V_{SSD(bord)4}$	35	–	digital border ground 4 (0 V)
$V_{DDD(bord)6}$	36	–	digital border supply voltage 6 (+5 V)
$V_{SSD(bord)5}$	37	–	digital border ground 5 (0 V)
PORT3	38	I/O	general purpose port 3 input/output (set via I^2C-bus)
PORT2	39	I/O	general purpose port 2 input/output (set via I^2C-bus)
PORT1	40	I/O	general purpose port 1 input/output (set via I^2C-bus)

SYMBOL	PIN	I/O	DESCRIPTION
PORT0	41	I/O	general purpose port 0 input/output (set via I^2C-bus)
$\overline{RES}$	42	I	reset input (active LOW for at least 30 clock cycles)
AP	43	I	connected to ground (action pin for testing)
SP	44	I	connected to ground (shift pin for testing)
FLDV	45	O	field identification output signal; VRAM port
VSYV	46	O	vertical sync output signal; VRAM port
HGTV	47	O	horizontal reference output signal; VRAM port
PXQV	48	O	pixel qualifier output signal to mark active pixels of a qualified line; VRAM port
BTST	49	I	connected to ground; BTST = HIGH sets all outputs to high-impedance state (testing)
VOEN	50	I	enable input signal for VRAM port
$V_{DDD(core)2}$	51	–	digital core supply voltage 2 (+3.3 V)
VMUX	52	I	VRAM output multiplexing, control input for the 32 to 16-bit multiplexer
$V_{SSD(core)2}$	53	–	digital core ground 2 (0 V)
HFL	54	O	FIFO half-full flag output signal
INCADR	55	O	line increment/vertical reset control output
VCLK	56	I/O	clock input/output signal for VRAM port
VRO31	57	O	32-bit digital VRAM port output (bit 31)
VRO30	58	O	32-bit digital VRAM port output (bit 30)
VRO29	59	O	32-bit digital VRAM port output (bit 29)
VRO28	60	O	32-bit digital VRAM port output (bit 28)
VRO27	61	O	32-bit digital VRAM port output (bit 27)
VRO26	62	O	32-bit digital VRAM port output (bit 26)
VRO25	63	O	32-bit digital VRAM port output (bit 25)
VRO24	64	O	32-bit digital VRAM port output (bit 24)
VRO23	65	O	32-bit digital VRAM port output (bit 23)
$V_{DDD(bord)7}$	66	–	digital border supply voltage 7 (+5 V)
$V_{SSD(bord)6}$	67	–	digital border ground 6 (0 V)
$V_{DDD(bord)8}$	68	–	digital border supply voltage 8 (+5 V)
$V_{SSD(bord)7}$	69	–	digital border ground 7 (0 V)
VRO22	70	O	32-bit VRAM port output (bit 22)
VRO21	71	O	32-bit VRAM port output (bit 21)
VRO20	72	O	32-bit VRAM port output (bit 20)
VRO19	73	O	32-bit VRAM port output (bit 19)
VRO18	74	O	32-bit VRAM port output (bit 18)
VRO17	75	O	32-bit VRAM port output (bit 17)
VRO16	76	O	32-bit VRAM port output (bit 16)
VRO15	77	O	32-bit VRAM port output (bit 15)
VRO14	78	O	32-bit VRAM port output (bit 14)
VRO13	79	O	32-bit VRAM port output (bit 13)
VRO12	80	O	32-bit VRAM port output (bit 12)

SYMBOL	PIN	I/O	DESCRIPTION
VRO11	81	O	32-bit VRAM port output (bit 11)
$V_{SSD(bord)8}$	82	–	digital border ground 8 (0 V)
$V_{DDD(bord)9}$	83	–	digital border supply voltage 9 (+5 V)
$V_{SSD(core)3}$	84	–	digital core ground 3 (0 V)
$V_{DDD(core)3}$	85	–	digital core supply voltage 3 (+3.3 V)
VRO10	86	O	32-bit VRAM port output (bit 10)
VRO9	87	O	32-bit VRAM port output (bit 9)
VRO8	88	O	32-bit VRAM port output (bit 8)
VRO7	89	O	32-bit VRAM port output (bit 7)
VRO6	90	O	32-bit VRAM port output (bit 6)
VRO5	91	O	32-bit VRAM port output (bit 5)
VRO4	92	O	32-bit VRAM port output (bit 4)
VRO3	93	O	32-bit VRAM port output (bit 3)
VRO2	94	O	32-bit VRAM port output (bit 2)
VRO1	95	O	32-bit VRAM port output (bit 1)
VRO0	96	O	32-bit VRAM port output (bit 0)
FDIO	97	I/O	field identification output signal; 7196 DIR input signal expansion port, I^2C-bus controlled
$V_{DDD(bord)10}$	98	–	digital border supply voltage 10 (+5 V)
$V_{SSD(bord)9}$	99	–	digital border ground 9 (0 V)
$V_{DDD(bord)11}$	100	–	digital border supply voltage 11 (+5 V)
$V_{SSD(bord)10}$	101	–	digital border ground 10 (0 V)
VIO	102	I/O	vertical sync input/output signal; expansion port
HIO	103	I/O	horizontal sync input/output signal; expansion port
PXQIO	104	I/O	pixel qualifier input/output signal to mark valid pixels; expansion port
VIDH7	105	I/O	bidirectional expansion port, high byte (bit 7) in 16-bit mode luminance component Y
VIDH6	106	I/O	bidirectional expansion port, high byte (bit 6) in 16-bit mode luminance component Y
VIDH5	107	I/O	bidirectional expansion port, high byte (bit 5) in 16-bit mode luminance component Y
VIDH4	108	I/O	bidirectional expansion port, high byte (bit 4) in 16-bit mode luminance component Y
VIDH3	109	I/O	bidirectional expansion port, high byte (bit 3) in 16-bit mode luminance component Y
VIDH2	110	I/O	bidirectional expansion port, high byte (bit 2) in 16-bit mode luminance component Y
VIDH1	111	I/O	bidirectional expansion port, high byte (bit 1) in 16-bit mode luminance component Y
VIDH0	112	I/O	bidirectional expansion port, high byte (bit 0) in 16-bit mode luminance component Y
$V_{DDD(bord)12}$	113	–	digital border supply voltage 12 (+5 V)

SYMBOL	PIN	I/O	DESCRIPTION
$V_{SSD(bord)11}$	114	–	digital border ground 11 (0 V)
$V_{DDD(core)4}$	115	–	digital core supply voltage 4 (+3.3 V)
$V_{SSD(core)4}$	116	–	digital core ground 4 (0 V)
VIDL7	117	I/O	bidirectional expansion port, low byte (bit 7) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL6	118	I/O	bidirectional expansion port, low byte (bit 6) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL5	119	I/O	bidirectional expansion port, low byte (bit 5) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL4	120	I/O	bidirectional expansion port, low byte (bit 4) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL3	121	I/O	bidirectional expansion port, low byte (bit 3) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL2	122	I/O	bidirectional expansion port, low byte (bit 2) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL1	123	I/O	bidirectional expansion port, low byte (bit 1) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL0	124	I/O	bidirectional expansion port, low byte (bit 0) in 16-bit mode time-multiplexed colour-difference components U and V
PXQIN	125	I	pixel qualifier input signal to mark valid pixels; expansion port
HIN	126	I	horizontal sync input signal; expansion port
VIN	127	I	vertical sync input signal; expansion port
LLCIO	128	I/O	line-locked system clock input/output; expansion port

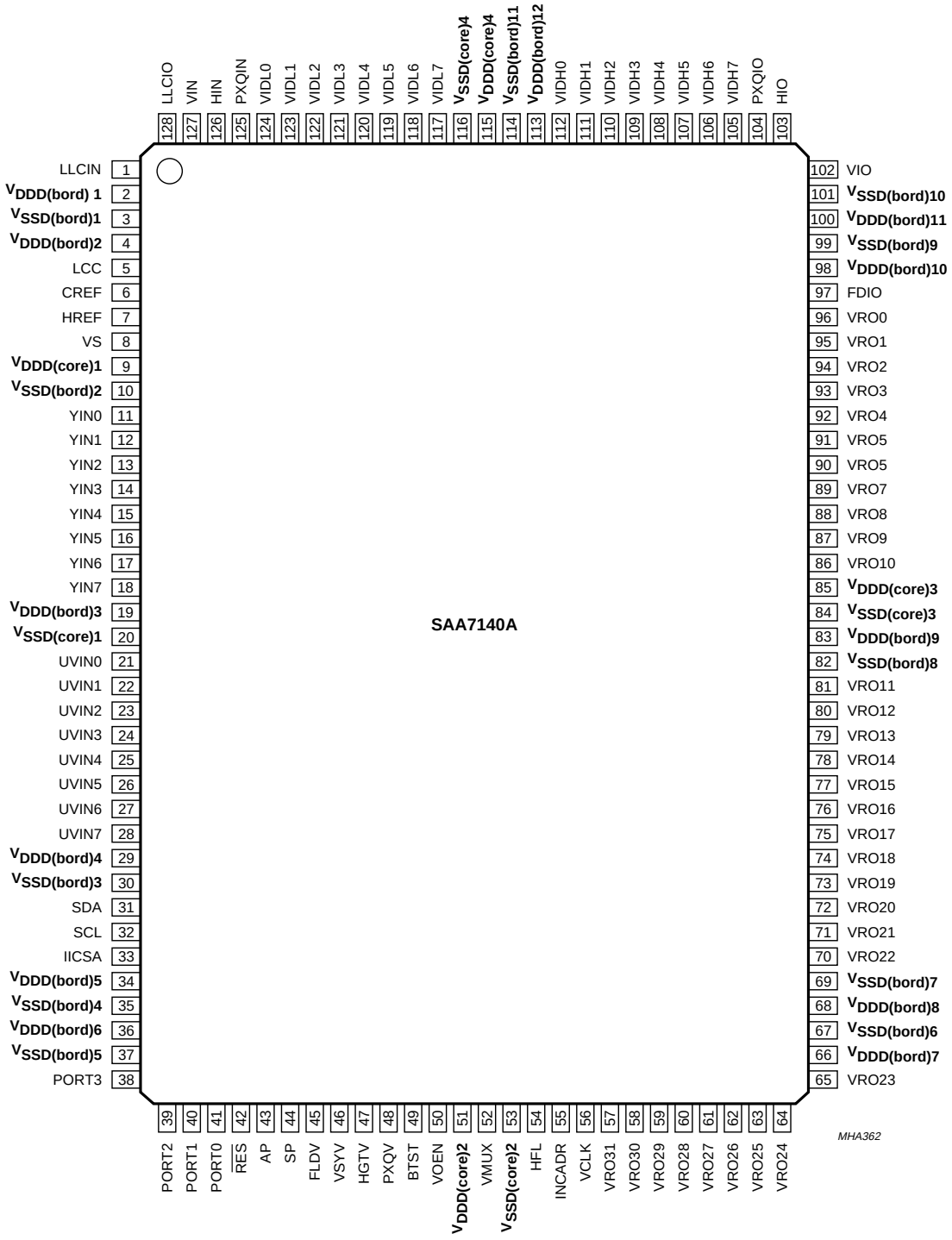


Fig.3 Pin configuration (SAA7140A).

6 PINNING (SAA7140B)

SYMBOL	PIN	I/O	DESCRIPTION
LLCIN	1	I	line-locked system clock input; expansion port
V_{DDD1}	2	–	digital supply voltage 1 (+3.3 V)
V_{SSD1}	3	–	digital ground 1 (0 V)
V_{DDD2}	4	–	digital supply voltage 2 (+3.3 V)
LLC	5	I	line-locked system clock input, maximum 32 MHz (2 × pixel rate); DMSD port
CREF	6	I	clock qualifier input (HIGH indicates valid input data YUV on DMSD port)
HREF	7	I	horizontal reference input signal; DMSD port
VS	8	I	vertical sync input signal; DMSD port
V_{DDD3}	9	–	digital supply voltage 3 (+3.3 V)
V_{SSD2}	10	–	digital ground 2 (0 V)
YIN0	11	I	luminance input data (bit 0); DMSD port
YIN1	12	I	luminance input data (bit 1); DMSD port
YIN2	13	I	luminance input data (bit 2); DMSD port
YIN3	14	I	luminance input data (bit 3); DMSD port
YIN4	15	I	luminance input data (bit 4); DMSD port
YIN5	16	I	luminance input data (bit 5); DMSD port
YIN6	17	I	luminance input data (bit 6); DMSD port
YIN7	18	I	luminance input data (bit 7); DMSD port
V_{DDD4}	19	–	digital supply voltage 4 (+3.3 V)
V_{SSD3}	20	–	digital ground 3 (0 V)
UVIN0	21	I	time-multiplexed colour-difference input data (bit 0); DMSD port
UVIN1	22	I	time-multiplexed colour-difference input data (bit 1); DMSD port
UVIN2	23	I	time-multiplexed colour-difference input data (bit 2); DMSD port
UVIN3	24	I	time-multiplexed colour-difference input data (bit 3); DMSD port
UVIN4	25	I	time-multiplexed colour-difference input data (bit 4); DMSD port
UVIN5	26	I	time-multiplexed colour-difference input data (bit 5); DMSD port
UVIN6	27	I	time-multiplexed colour-difference input data (bit 6); DMSD port
UVIN7	28	I	time-multiplexed colour-difference input data (bit 7); DMSD port
V_{DDD5}	29	–	digital supply voltage 5 (+3.3 V)
V_{SSD4}	30	–	digital ground 4 (0 V)
SDA	31	I/O	serial data input/output (I^2C-bus)
SCL	32	I	serial clock input (I^2C-bus)
IICSA	33	I	set address input (I^2C-bus)
V_{DDD6}	34	–	digital supply voltage 6 (+3.3 V)
V_{SSD5}	35	–	digital ground 5 (0 V)
V_{DDD7}	36	–	digital supply voltage 7 (+3.3 V)
V_{SSD6}	37	–	digital ground 6 (0 V)
PORT3	38	I/O	general purpose port 3 input/output (set via I^2C-bus)
PORT2	39	I/O	general purpose port 2 input/output (set via I^2C-bus)
PORT1	40	I/O	general purpose port 1 input/output (set via I^2C-bus)

SYMBOL	PIN	I/O	DESCRIPTION
PORT0	41	I/O	general purpose port 0 input/output (set via I^2C-bus)
$\overline{RES}$	42	I	reset input (active LOW for at least 30 clock cycles)
AP	43	I	connected to ground (action pin for testing)
SP	44	I	connected to ground (shift pin for testing)
FLDV	45	O	field identification output signal; VRAM port
VSYV	46	O	vertical sync output signal; VRAM port
HGTV	47	O	horizontal reference output signal; VRAM port
PXQV	48	O	pixel qualifier output signal to mark active pixels of a qualified line; VRAM port
BTST	49	I	connected to ground; BTST = HIGH sets all outputs to high-impedance state (testing)
VOEN	50	I	enable input signal for VRAM port
$\mathbf{V_{DDD8}}$	51	–	digital supply voltage 8 (+3.3 V)
VMUX	52	I	VRAM output multiplexing, control input for the 32 to 16-bit multiplexer
$\mathbf{V_{SSD7}}$	53	–	digital ground 7 (0 V)
HFL	54	O	FIFO half-full flag output signal
INCADR	55	O	line increment/vertical reset control output
VCLK	56	I/O	clock input/output signal for VRAM port
VRO31	57	O	32-bit digital VRAM port output (bit 31)
VRO30	58	O	32-bit digital VRAM port output (bit 30)
VRO29	59	O	32-bit digital VRAM port output (bit 29)
VRO28	60	O	32-bit digital VRAM port output (bit 28)
VRO27	61	O	32-bit digital VRAM port output (bit 27)
VRO26	62	O	32-bit digital VRAM port output (bit 26)
VRO25	63	O	32-bit digital VRAM port output (bit 25)
VRO24	64	O	32-bit digital VRAM port output (bit 24)
VRO23	65	O	32-bit digital VRAM port output (bit 23)
$\mathbf{V_{DDD9}}$	66	–	digital supply voltage 9 (+3.3 V)
$\mathbf{V_{SSD8}}$	67	–	digital ground 8 (0 V)
$\mathbf{V_{DDD10}}$	68	–	digital supply voltage 10 (+3.3 V)
$\mathbf{V_{SSD9}}$	69	–	digital ground 9 (0 V)
VRO22	70	O	32-bit VRAM port output (bit 22)
VRO21	71	O	32-bit VRAM port output (bit 21)
VRO20	72	O	32-bit VRAM port output (bit 20)
VRO19	73	O	32-bit VRAM port output (bit 19)
VRO18	74	O	32-bit VRAM port output (bit 18)
VRO17	75	O	32-bit VRAM port output (bit 17)
VRO16	76	O	32-bit VRAM port output (bit 16)
VRO15	77	O	32-bit VRAM port output (bit 15)
VRO14	78	O	32-bit VRAM port output (bit 14)
VRO13	79	O	32-bit VRAM port output (bit 13)
VRO12	80	O	32-bit VRAM port output (bit 12)

SYMBOL	PIN	I/O	DESCRIPTION
VRO11	81	O	32-bit VRAM port output (bit 11)
V_{SSD10}	82	–	digital ground 10 (0 V)
V_{DDD11}	83	–	digital supply voltage 11 (+3.3 V)
V_{SSD11}	84	–	digital ground 11 (0 V)
V_{DDD12}	85	–	digital supply voltage 12 (+3.3 V)
VRO10	86	O	32-bit VRAM port output (bit 10)
VRO9	87	O	32-bit VRAM port output (bit 9)
VRO8	88	O	32-bit VRAM port output (bit 8)
VRO7	89	O	32-bit VRAM port output (bit 7)
VRO6	90	O	32-bit VRAM port output (bit 6)
VRO5	91	O	32-bit VRAM port output (bit 5)
VRO4	92	O	32-bit VRAM port output (bit 4)
VRO3	93	O	32-bit VRAM port output (bit 3)
VRO2	94	O	32-bit VRAM port output (bit 2)
VRO1	95	O	32-bit VRAM port output (bit 1)
VRO0	96	O	32-bit VRAM port output (bit 0)
FDIO	97	I/O	field identification output signal; 7196 DIR input signal expansion port, I^2C-bus controlled
V_{DDD13}	98	–	digital supply voltage 13 (+3.3 V)
V_{SSD12}	99	–	digital ground 12 (0 V)
V_{DDD14}	100	–	digital supply voltage 14 (+3.3 V)
V_{SSD13}	101	–	digital ground 13 (0 V)
VIO	102	I/O	vertical sync input/output signal; expansion port
HIO	103	I/O	horizontal sync input/output signal; expansion port
PXQIO	104	I/O	pixel qualifier input/output signal to mark valid pixels; expansion port
VIDH7	105	I/O	bidirectional expansion port, high byte (bit 7) in 16-bit mode luminance component Y
VIDH6	106	I/O	bidirectional expansion port, high byte (bit 6) in 16-bit mode luminance component Y
VIDH5	107	I/O	bidirectional expansion port, high byte (bit 5) in 16-bit mode luminance component Y
VIDH4	108	I/O	bidirectional expansion port, high byte (bit 4) in 16-bit mode luminance component Y
VIDH3	109	I/O	bidirectional expansion port, high byte (bit 3) in 16-bit mode luminance component Y
VIDH2	110	I/O	bidirectional expansion port, high byte (bit 2) in 16-bit mode luminance component Y
VIDH1	111	I/O	bidirectional expansion port, high byte (bit 1) in 16-bit mode luminance component Y
VIDH0	112	I/O	bidirectional expansion port, high byte (bit 0) in 16-bit mode luminance component Y
V_{DDD15}	113	–	digital supply voltage 15 (+3.3 V)

SYMBOL	PIN	I/O	DESCRIPTION
V_{SSD14}	114	–	digital ground 14 (0 V)
V_{DDD16}	115	–	digital supply voltage 16 (+3.3 V)
V_{SSD15}	116	–	digital ground 15 (0 V)
VIDL7	117	I/O	bidirectional expansion port, low byte (bit 7) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL6	118	I/O	bidirectional expansion port, low byte (bit 6) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL5	119	I/O	bidirectional expansion port, low byte (bit 5) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL4	120	I/O	bidirectional expansion port, low byte (bit 4) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL3	121	I/O	bidirectional expansion port, low byte (bit 3) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL2	122	I/O	bidirectional expansion port, low byte (bit 2) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL1	123	I/O	bidirectional expansion port, low byte (bit 1) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL0	124	I/O	bidirectional expansion port, low byte (bit 0) in 16-bit mode time-multiplexed colour-difference components U and V
PXQIN	125	I	pixel qualifier input signal to mark valid pixels; expansion port
HIN	126	I	horizontal sync input signal; expansion port
VIN	127	I	vertical sync input signal; expansion port
LLCIO	128	I/O	line-locked system clock input/output; expansion port

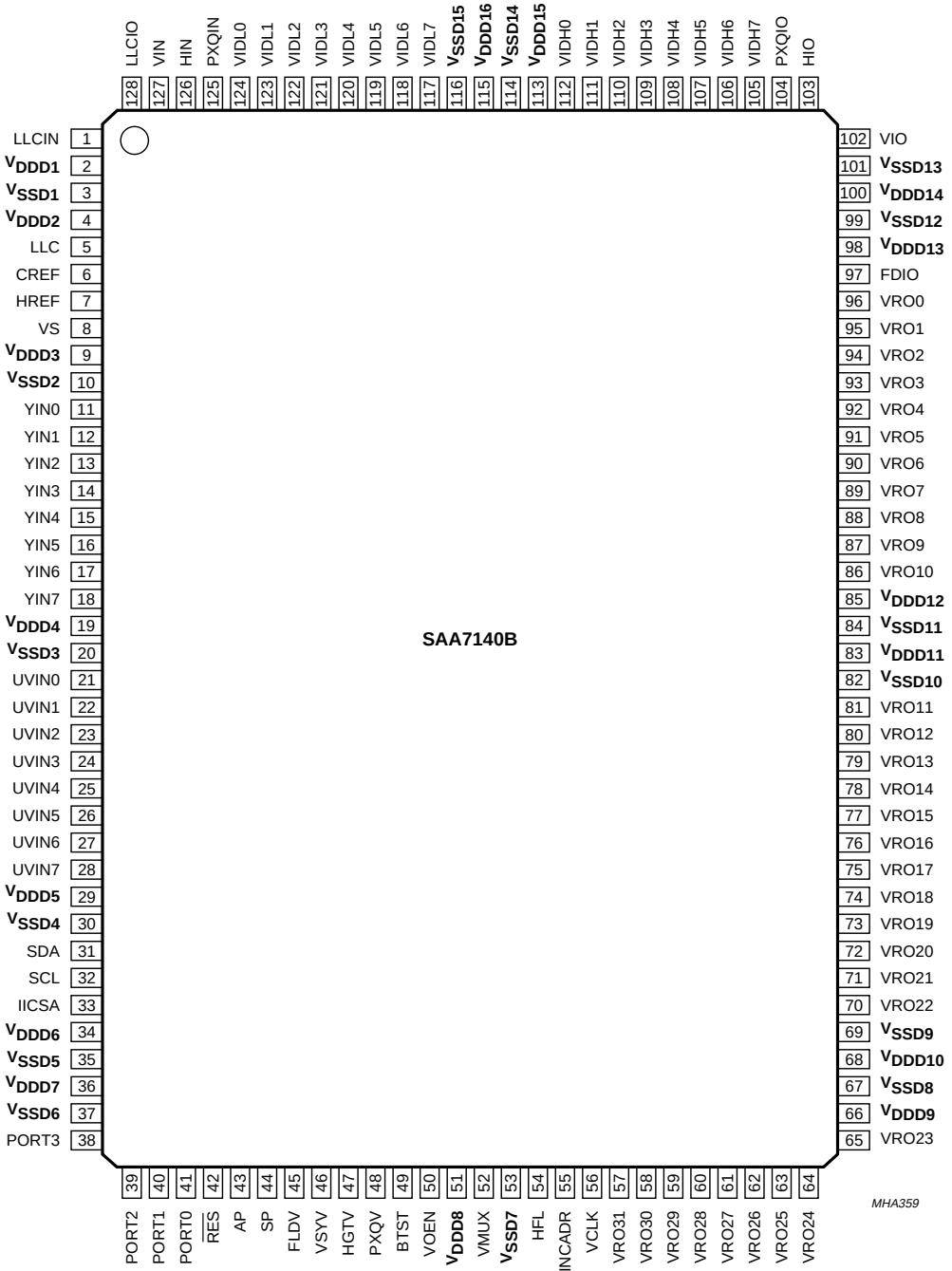


Fig.4 Pin configuration (SAA7140B).

7 FUNCTIONAL DESCRIPTION

The SAA7140A and SAA7140B accepts YUV data in a 16-bit wide parallel format at the DMSD port and accepts YUV input in a 16-bit wide parallel format and in an 8-bit byte-multiplexed Cb-Y-Cr-Y- format (CCIR-656 or D1 oriented) at the expansion port.

Depending on the selected port modes, the incoming data is formatted to the internal data representation, where reference signals or codes are detected in the Data Formatter/Reformatter (DFR). The horizontal and vertical timing reference can be defined under I^{2}C-bus control. Based on that timing reference, the active processing window is defined in a versatile way via the programming. Two programming sets can be loaded simultaneously, and become valid for processing in a field alternating way. Before being processed in the central scaling unit, the incoming data passes through the BCS control unit where monitor control functions, for adjusting brightness, contrast (luminance) and saturation (chrominance) are implemented.

The scaling is performed in three steps:

1. Horizontal prescaling (bandwidth limitation for anti-aliasing, via FIR prefiltering and subsampling)
2. Vertical scaling (generating phase interpolated or vertically low-passed lines)
3. Horizontal variable phase scaling (phase-correct scaling to the new geometric relationships).

The scaled output data is fed back to the DFR unit and may be used as output signals from the bidirectional expansion port (if the mode is selected). They are converted in parallel from the YUV to the RGB domain in a digital matrix. Anti-gamma correction of gamma-corrected input signals can be performed in the RGB data path. The output formatter then formats the scaled data to one of the various output formats (e.g. monochrome, 16-bit YUV or 32-bit RGB (5, 5, 5).

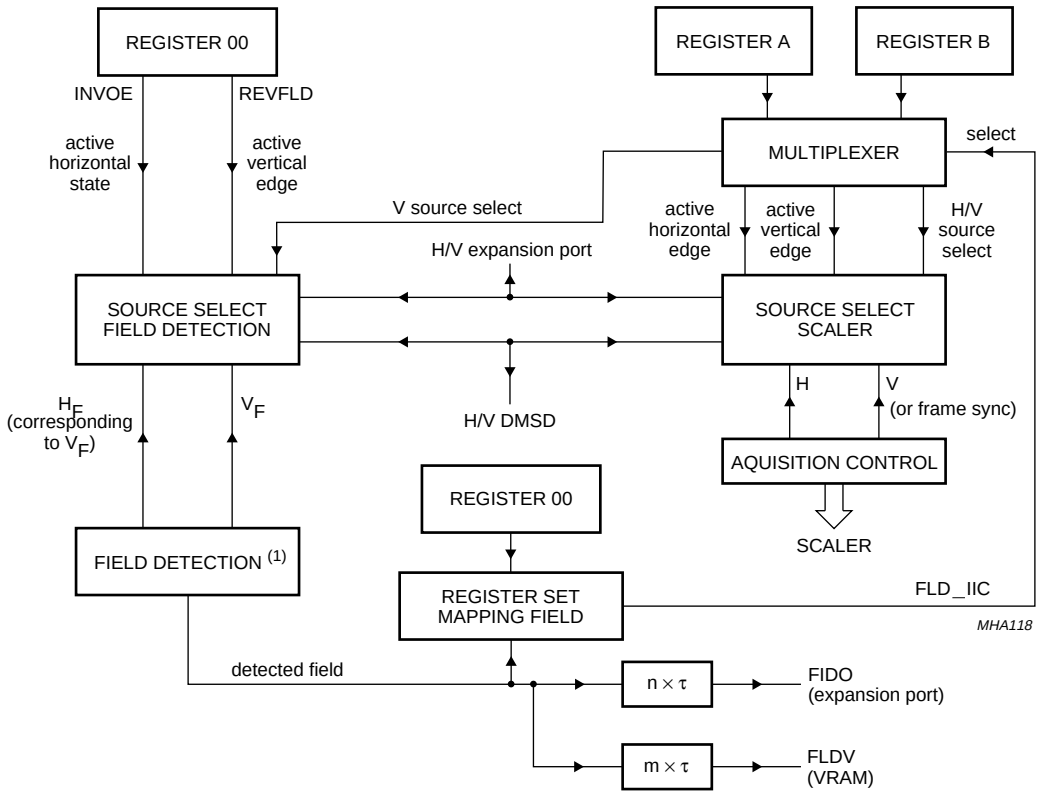
To ease frame buffer applications, the data can be transferred in a synchronous way (transparent mode), using separate reference and qualifier signals and a continuous output clock (VCLK). The data can also be transferred in an asynchronous way (burst mode) using the HFL and INCADR flags and a discontinuous input clock burst on VCLK.

In a typical application, the 16-bit wide YUV input receives clock, sync and data from a video decoder (SAA71xx) via the DMSD port. An MPEG compression/decompression circuit can be connected at the expansion port to receive the decoder data, scaled or unscaled, or to deliver data to the scaling processor. The scaling operation of the SAA7140A and SAA7140B can be performed on the data from a video decoder, or on the data from the MPEG-codec at the expansion port input. The source selection can be static or toggled on a field-by-field basis. For example, during the odd field the video decoder signal is scaled in accordance with the ‘odd’ parameter set for display in a window. The compression codec receives unscaled data. During the even field the decompressed data from the MPEG decoder gets sized for a second display window in accordance with the ‘even’ parameter set. The resulting output from the scaling operation is delivered via the 32-bit wide output (VRAM port) and to the expansion port output (optional).

7.1 Data format/reformatter and reference signal generation

The video data can be formatted/reformatted in accordance with the selected expansion port mode, from 16-bit (DMSD port) to serial 8-bit (expansion port output), from serial 8-bit (expansion port input) to internal parallel 16-bit format and from 24-bit (scaler output) to 16-bit/8-bit respectively (expansion port output). The definition of the timing references for the acquisition and field detection (polarity and edge selection) are based on the selected reference signal source. The field detector regenerates the field information from the selected incoming reference signals (see Fig.5).

The field sequence flag (FLD), detects the state of the H-sync signal at the reference edge of the V-sync signal. The detection is controlled by I^{2}C-bus bits REVFLD and INVOE. The detection output can be seen on pins FLDV and FDIO (if FLDC = 0). Bits IREGS and SREGS control the mapping of the detected sequence to the I^{2}C-bus register sets A and B (I^{2}C-bus subaddress 02 to 1F and 22 to 3F).



FLD detection modes (I²C-bus bits FICO1 and FICO0);

(1) In the normal mode: the FLD signal is detected from the incoming H and V signals.

In the improved mode: the FLD signal is resynchronized only after the H and V sequence runs stable for a certain period of time.

In the force toggle mode: the FLD signal toggles with every event on the V signal (H is independent).

Register set mapping modes (I²C-bus bits IREGS and SREGS);

The FLD_IIC signal carries the detected FLD or the inverted FLD.

The signal is fixed to 0 (Register set A forced) or forced to 1 (Register set A forced).

Fig.5 Field detection/register set mapping.

7.1.1 Data formats and reference signals of the DMSD port

The 16-bit YUV colour difference and luminance signals (straight binary) are available in parallel on a 16-bit wide data stream. The code is in accordance with CCIR-601; black = 16, white = 235, no colour = 128, 100% colour saturation = 16 to 240 etc. Overshoots and undershoots are permitted and supported, i.e. processed as they are. The 16-bit wide YUV data format from the DMSD port (input only) is defined with Line-Locked Clock (LLC) with a double pixel clock frequency. Every second clock cycle is qualified with CREF, in pixel rate frequency.

The internal processing of the SAA7140A and SAA7140B relies on the presence of LLC, i.e. a clock of at least twice the sampling rate of the input data stream. The maximum LLC rate is 32 MHz.

The horizontal sync input (HREF) may be supplied as a H-pulse or horizontal gate signal. The positive or negative edge, (programmable by I²C-bus bit REHAW), indicates the horizontal timing reference. The first valid pixels may occur not exactly at the start of the line but with a certain offset (counted in qualified pixels).

The vertical timing is indicated by the positive or negative edge (programmable by I²C-bus bit REVAW) of the sync input signal VS. The first valid line may occur not exactly at the start of the field but with a certain offset, counted in lines, with qualified pixels. Input signal VS defines, in relation to HREF, the odd/even field detection (see *SAA7191B*).

7.1.2 Data formats and reference signals of the expansion port

The expansion port (input/output) supports several modes; simultaneous (parallel) D1 input and D1 output (full duplex) with auxiliary sync and qualifying signals, or 16-bit wide YUV input or output (half duplex), selected via programming with clock, qualify and sync signal.
A discontinuous data stream is supported by accepting or generating a pixel/byte qualifying signal (PXQ), a generalization of the CREF definition at the DMSD port (PXQ = 1 qualified pixel, PXQ = 0 invalid data).

16-bit YUV (half duplex mode = field alternating data I/O): 16-bit YUV data stream (Y = VIDH7 to VIDH0, UV = VIDL7 to VIDL0). For the 16-bit YUV data input format, PXQ is inhibited from qualifying adjacent LLC clock cycles. There must be at least one empty clock cycle between two valid pixels.

8-bit Cb-Y-Cr-Y; CCIR 656 or D1 (full duplex mode): the colour difference signals and the luminance signal (straight binary) are byte-wise multiplexed onto the same 8-bit wide data stream, with sequence and timing in accordance with CCIR 656 recommendations (according to D1 for 60 Hz application respectively). The code is in accordance with CCIR 601 (black = 16, white = 235, no colour = 128, 100% colour saturation = 16 or 240, etc. Overshoots and undershoots are permitted and supported, i.e. processed as they are.

If the CCIR 656 output is selected, the video signal is clipped to 01H and FEH in order to leave the codes 00H and FFH for SAV and EAV encoding (SAV and EAV encoding not yet supported). The clock rate for this format is twice the pixel clock.

The horizontal sync input HIN is processed in an identical manner to HREF at the DMSD port. If the CCIR 656 data input format is selected, the horizontal timing reference is decoded from the input data stream (SAV, EAV and SHVS = 1) or taken from the selected H-reference signal HIN, HREF or HIO (SHVS = 0). The start condition to enable synchronization to the correct Cb-Y-Cr-Y-sequence is provided by the selected horizontal reference signal. The sequence only increments with qualified bytes.

Instead of a vertical sync signal, as described for the DMSD port, the expansion port also supports an odd/even signal applied to the input pin VIN or VIO (controlled by I²C-bus bit FSEL). The frame and the field timing is then indicated by a positive or negative edge of the V input. This may occur with a certain offset at the frame and field start, and is normally counted in lines.

If the CCIR 656 data input format is selected, the vertical timing reference is decoded from the input data stream by SAV and EAV (SHVS = 1) or taken from the selected V reference signal VIN, VS or VIO (SHVS = 0). The vertical synchronization pin can be programmed to carry either a vertical sync signal or an odd/even signal.

The horizontal and vertical sync outputs HIO and VIO are expansion port mode dependent and can be selected via the I²C-bus (VD1/VD0 and HD1/HD0):

Should the DMSD port be selected as the output source, HIO will carry a copy of HREF and VIO will carry a copy of VS.

If the expansion port carries data from the scaler output, then HIO is a gate signal enveloping the range of active video along a line and VIO is a positive sync pulse with a length of 4 lines

If HIN/VIN is selected as the output source, HIO carries a copy of HIN and VIO carries a copy of VIN (short cut).

If the CCIR 656 data output format is selected, the horizontal and vertical sync output signals are only supplied at pins HIO and VIO (SAV and EAV are not encoded as outputs).

Due to compatibility reasons to the expansion port definition of the SAA7194/SAA7196 circuits, the bidirectional pins HIO, VIO and PXQIO can also be configured as input pins (see Table 3).

The definition of the pin FDIO is I²C-bus selectable. Configured as an output pin, FDIO carries an odd/even signal generated in the FLD detection (see Fig.5). Configured as an input pin, FDIO controls the direction of the expansion port (compatibility to SAA7194/SAA7196, (see Table 3 and Chapter 8).

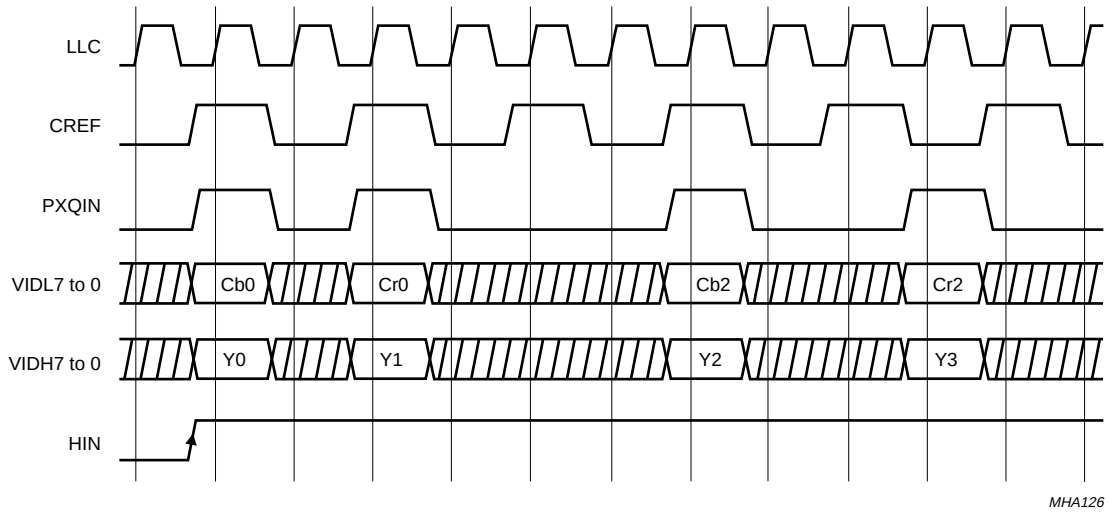


Fig.6 Timing of PXQIN for 16-bit data input from DMSD to expansion port.

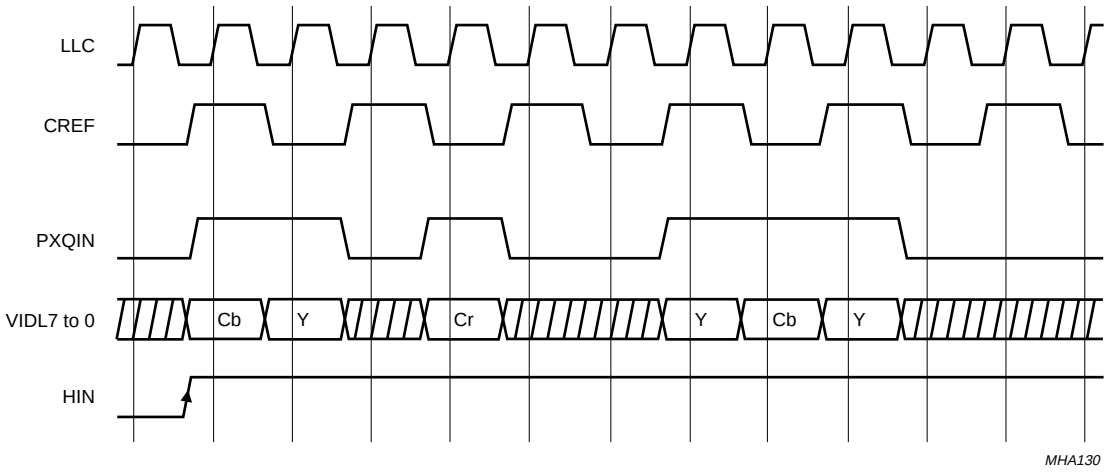


Fig.7 Timing of PXQIO for serial 8-bit data input at expansion port.

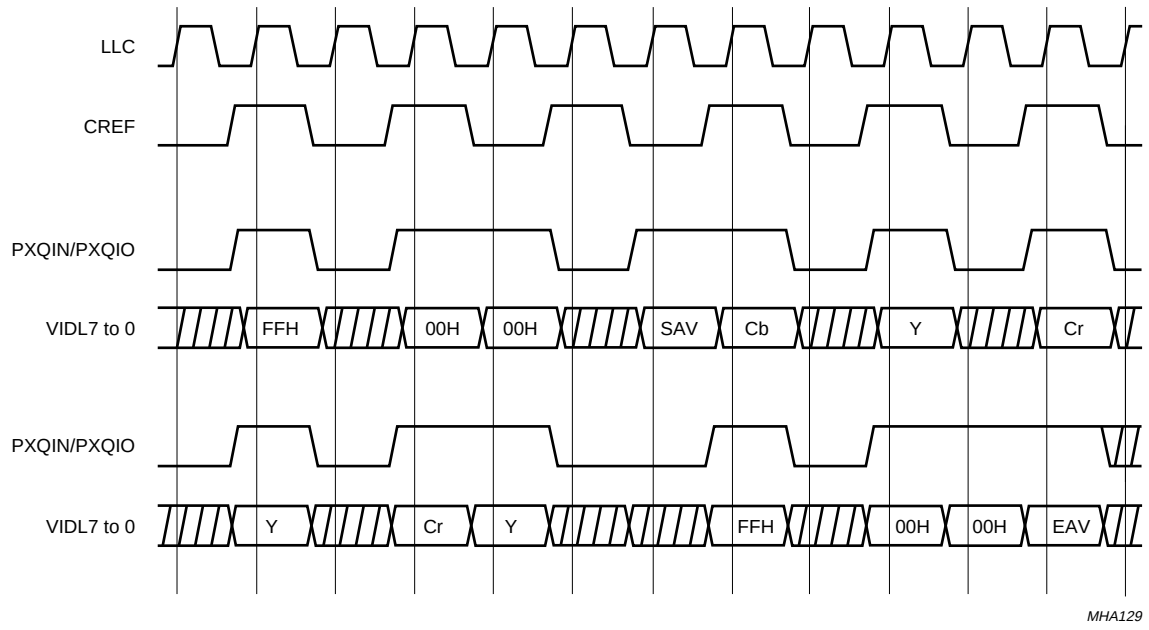


Fig.8 Timing of PXQIN/PXQIO for CCIR 656 data input at expansion port.

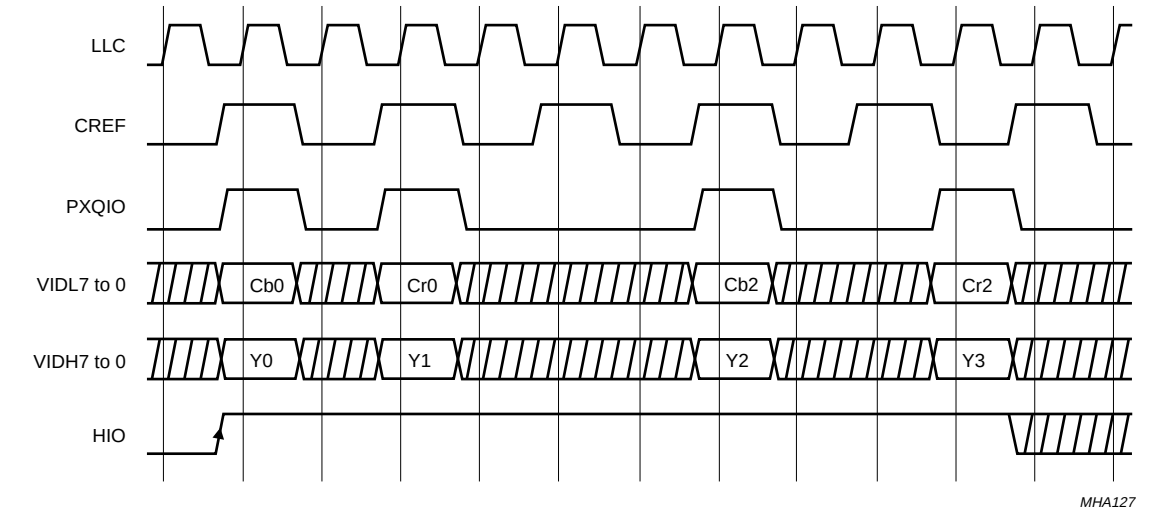


Fig.9 Timing of PXQIO for non-zoomed 16-bit data output at expansion port.

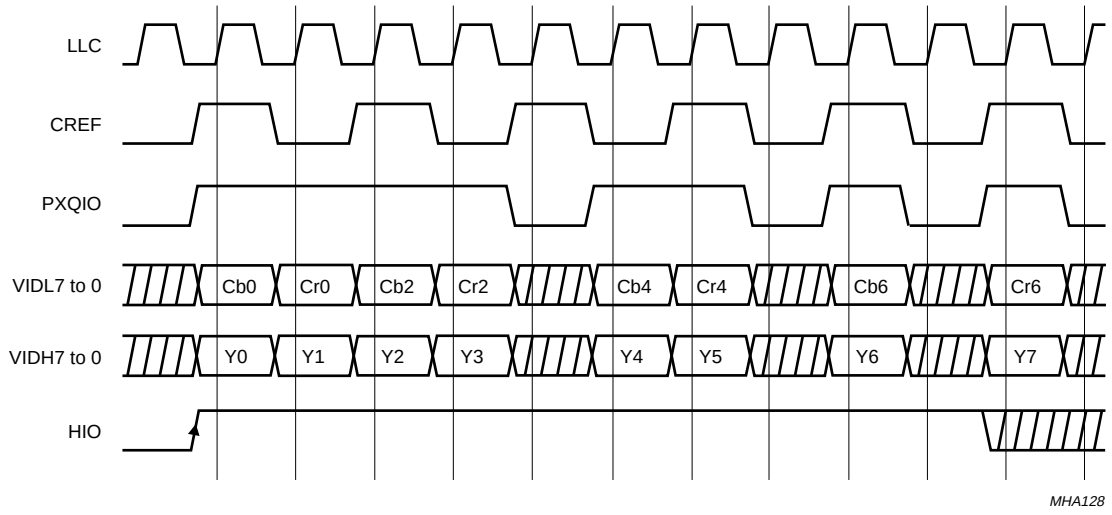


Fig.10 Timing of PXQIN for zoomed 16-bit data output at expansion port.

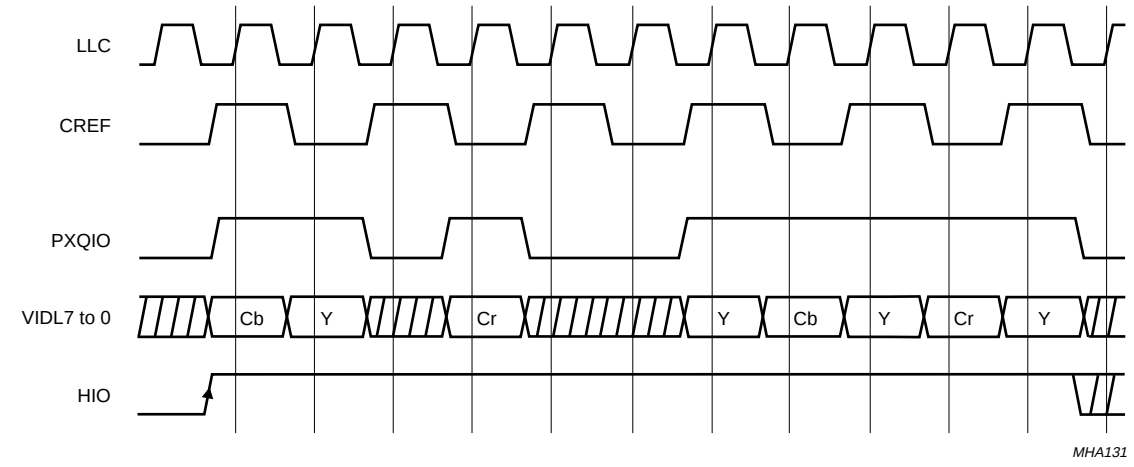
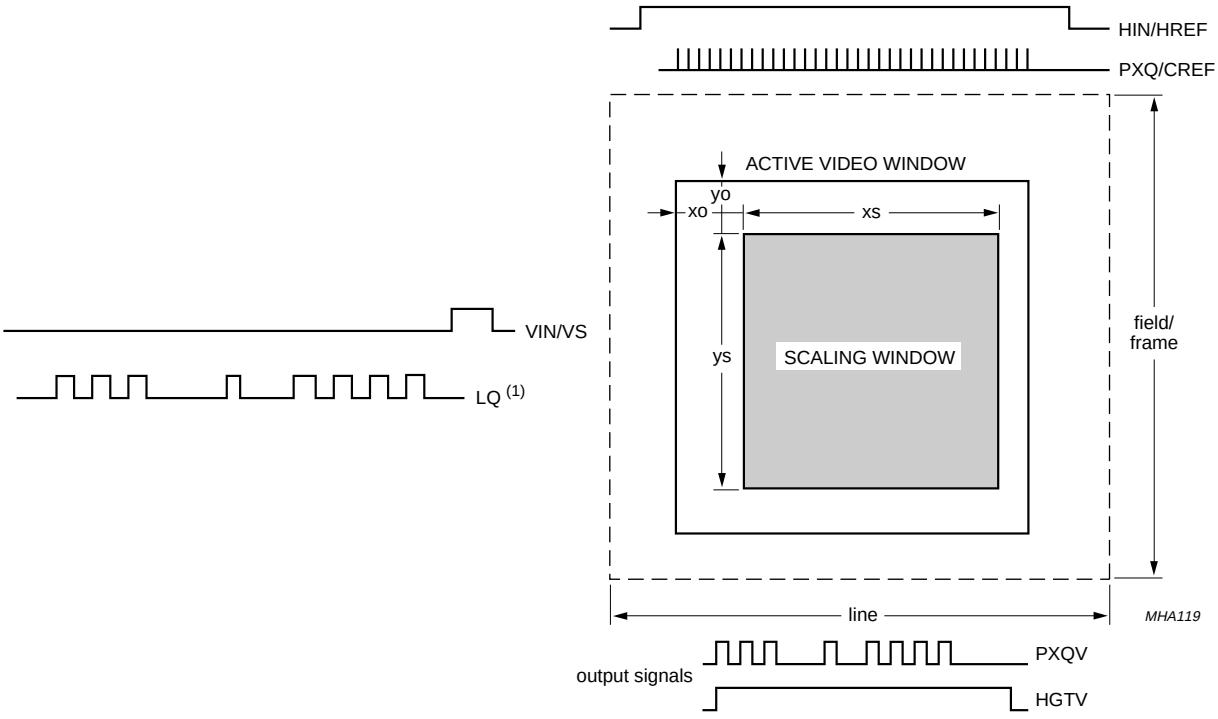


Fig.11 Timing of PXQIO for serial 8-bit data output at expansion port.

7.2 Acquisition control

The processing window for the scaling unit is defined in the acquisition control unit. An internal counter receives I²C-bus controlled values for offset (bits XO10 to XO0 and YO10 to YO0) and length (bits XS10 to XS0 and YS10 to YS0). The counter is reset by the corresponding sync reference input signal. The horizontal counter increments in qualified pixels and the vertical counter increments in qualified lines, i.e. lines containing at least one qualified pixel. Depending on the selected mode, the source for the horizontal reference may be HREF (DMSD port) or HIN (expansion port), or for the vertical reference, VS (DMSD port) or VIN (expansion port).

It should be noted that in order to avoid programming dependent line and field drop effects, all values must not exceed the number of qualified pixels per line or lines per field.



(1) LQ = qualified lines i.e. lines containing at least one qualified pixel.

Fig.12 Reference signals for scaling window.

7.3 BCS control

The parameters for Brightness, Contrast and Saturation (BSC) can be adjusted in the BSC control unit.

The luminance signal can be controlled via the I²C-bus using bits BRIG7 to BRIG0 and CONT6 to CONT0.

For the brightness control:

00H = minimum offset

80H = nominal level

FFH = maximum offset.

For the contrast control:

00H = luminance off

40H = nominal gain of 1.01

7FH = maximum gain of 1.9999.

The chrominance signal can be controlled via the I²C-bus using bits SAT6 to SAT0.

For the saturation control:

00H = colour off

40H = nominal gain of 1.0

7FH = maximum gain of 1.9999.

With respect to limiting, all values are limited to minimum (equals 0) and maximum (equals 255).

7.4 Scaling unit

Scaling to a randomly sized window is performed in three steps:

1. Horizontal prescaling (bandwidth limitation for anti-aliasing, via FIR prefiltering and subsampling)
2. Vertical scaling (generating phase interpolated or vertically low-passed lines)
3. Horizontal variable phase scaling (phase-correct scaling to the new geometric relations).

The scaling processor can obtain its clock from the DMSD port or the expansion port. Normally the two ports are synchronized to support program-set-swapping, asynchronous working results in restricted operation. The video signal source also provides the source for the scalers qualify signal PXQ.

The scaling process generates a new pixel/clock qualifier sequence. This results in PXQ being used at the VRAM port in the transparent mode, and for the expansion port output. There are restrictions in the combination of the input sample rate and up or down-scaling mode and scaling factor. The maximum resulting output sample rate at the VRAM port is LLC and at the expansion port the maximum pixel rate is ½LLC, due to the support of the CCIR 656 format.

7.4.1 HORIZONTAL PRESCALING

The incoming pixels in the selected range are preprocessed in the horizontal prescaler, which is the first stage of the scaling unit. The prescaler consists of an FIR prefilter and a pixel collecting subsampler.

7.4.1.1 FIR prefilter

The video components Y, U and V are FIR prefiltered to reduce the signal bandwidth in accordance with the downscale for factors between 1 to ½, thus aliasing due to signal bandwidth expansion is reduced.

The prefilter consists of 3 filter stages. The transfer functions are given in Chapter 8.
The prefilter is controlled by the I²C-bus bits PFY3 to 0 and PFUV3 to 0 in I²C-bus subaddress 13 and 33.

Figures 13 and 14 illustrate some frequency responses and the corresponding I²C-bus settings.
The prefilter operates on 4 : 4 : 4 YUV data. As U and V are generated by simple chroma pixel doubling, the UV prefilter should also be used to generate the interpolated chroma values.

7.4.1.2 Subsampler

To improve the scaling performance for scales of less than ½ down to icon size, a FIR filtering subsampler is available. It performs a subsampling of the incoming data by a factor of 1/N (where N = XPSC + 1 = 1 to 64). With N_{IP} equalling the number of input pixel/line and N_{OP} equalling the number of desired output pixels/line, the basic equation to calculate XPSC is as follows:

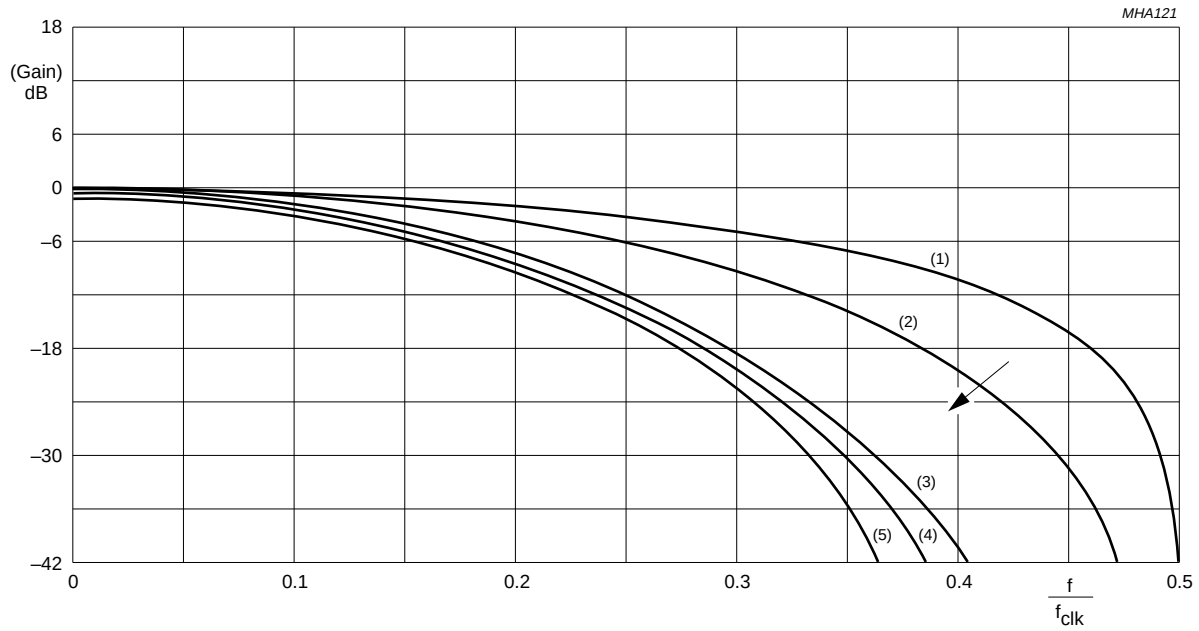
$$XPSC = TRUNC \times \left(\frac{N_{IP}}{N_{OP} - 1} \right)$$

The subsampler collects a number of [N + 1(–XACM)] pixels to calculate a new subsampled output pixel. Consequently, a downscale dependent FIR filter has been incorporated, with up to 65 taps, which reduces aliasing for small sizes. If XACM = 0 the collecting sequence overlaps, which means that the last pixel of sequence M is also the first pixel of sequence M + 1. To implement a real subsampler bypass XACM has to be set to logic 1.

It should be noted that because the phase-correct horizontal fine scaling is limited to a maximum downscale of ¼, this circuitry has to be used for downscales less than ¼ of the incoming pixel count.

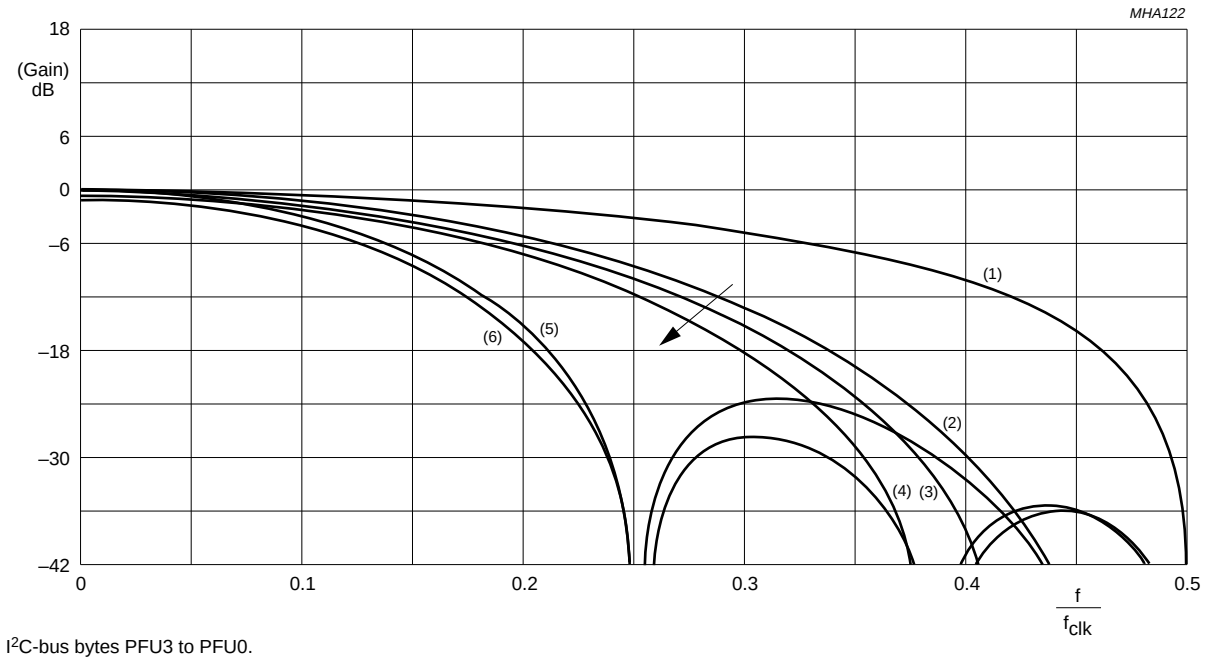
To obtain unity gain at the subsamplers output for all subsampling ratios, the I²C-bus parameters CXY, CXUV and DCGX have to be used. In addition, the I²C-bus parameters can be used to slightly modify the FIR characteristic of the subsampler.

Table 1 gives examples of I²C-bus register settings, depending on a given prescaler ratio. With reference to Table 1, it should be noted that an internal XPSC-dependent automatic prenormalization becomes valid for XPSC > 8, > 6 and >32, which reduces the input signal quantization. In addition, for XPSC ≥ 15 the LSB of the CXY and CXUV parameter become valid.



I²C-bus bytes PFY3 to PFY0.
(1) = 0001; (2) = 0010; (3) = 0011; (4) = 1011; (5) = 1111.

Fig.13 Luminance prefilter frequency response for miscellaneous I²C-bus settings.



I²C-bus bytes PFU3 to PFU0.
(1) = 0001; (2) = 0010; (3) = 1010; (4) = 1110; (5) = 0011; (6) = 1111.

Fig.14 Chrominance prefilter frequency response for miscellaneous I²C-bus settings.

Table 1 Horizontal prescaling and normalization

HORIZONTAL PRESCALING	XPSC	COEFFICIENT SEQUENCE (example)	CXY (luma)/ CXUV (chroma) (HEX)	WEIGHT SUM	DCGX	BSC (CONT/SAT) = x/y × 64
1	0	1-1	00	2	1	1
1/2	1	1-1-1	00	3	1	2/3
		1-2-1	02	4	2	1
1/3	2	1-1-1-1	00	4	2	1
1/4	3	1-1-1-1-1	00	5	2	4/5
		1-2-2-2-1	06	8	3	1
1/5	4	111 111	00	6	2	4/6
		121 121	02	8	3	1
		112 211	04	8	3	1
1/6	5	111 1 111	00	7	3	8/7
		111 2 111	08	8	3	1
1/7	6	1111 1111	00	8	3	1
1/8	7	1111 1 1111	00	9	3	8/9
		1222 2 2221	1E	16	7	1
1/9	8	1111 1 1 1111	00	10/2	2	4/5
		1221 2 2 1221	16	16/2	3	1
		1122 2 2 2211	1C	16/2	3	1
1/10	9	1111 1 1 1 1111	00	11/2	2	8/11
		1212 1 2 1 2121	2A	16/2	3	1
		1112 2 2 2 2111	38	16/2	3	1
1/11	10	1111 11 11 1111	00	12/2	2	8/12
		1211 21 12 1121	12	16/2	3	1
		1111 22 22 1111	30	16/2	3	1
1/12	11	1111 11 1 11 1111	00	13/2	2	8/13
		1121 11 2 11 1211	44	16/2	3	1
		1111 12 2 21 1111	60	16/2	3	1
1/13	12	1111 111 111 1111	00	14/2	2	8/14
		1111 211 112 1111	10	16/2	3	1
		1111 112 221 1111	40	16/2	3	1
1/14	13	1111 111 1 111 1111	00	15/2	2	8/15
		1111 111 2 111 1111	80	16/2	3	1
1/15	14	1111 1111 1111 1111	00	16/2	3	1
1/16	15	1111 1111 1 1111 1111		17/2	3	16/17
		1222 2222 2 2222 2221	FF	32/2	7	1
1/17	16	1111 1111 1 1 1111 1111	00	18/4	2	16/18
		1222 2222 1 1 2222 2221	FE	32/4	3	1
		1222 2122 22 2212 2221	DF	32/4	3	1

HORIZONTAL PRESCALING	XPSC	COEFFICIENT SEQUENCE (example)	CXY (luma)/ CXUV (chroma) (HEX)	WEIGHT SUM	DCGX	BSC (CONT/SAT) = x/y × 64
1/18	17	1111 1111 1 1 1 1111 1111	00	19/4	2	16/19
		1222 1222 1 2 1 2221 2221	EE	32/4	3	1
		1222 2112 2 2 2 2112 2221	9F	32/4	3	1
....	....	....	....	xx/4	....	....
1/33	32	1111 ... 1111	00	34/8	2	–
....	....	....	....	xx/8	....	....
1/63	62	....	....	....	....	....
1/64	63	....	....	....	....	....

7.4.2 VERTICAL SCALER

The vertical scaler performs the vertical downscaling of the input data stream to a random number of output lines. It can be used for input line lengths up to 768 pixels/line and has to be bypassed if the input line length exceeds the pixel count.

For vertical scaling there are two different modes implemented; the ACCU mode (vertical accumulation) for scales down to icon size and the Linear Phase Interpolation mode (LPI) for scales between 1 and 1/2.

7.4.2.1 ACCU mode (scaling factor range 1 to 1/1024; I²C-bus bit YACM = 1:

The ACCU mode can be used for vertical scaling down to icon size. In this mode, the I²C-bus parameter YSCI controls the scaling and parameter YACL controls the vertical anti-alias filtering.

The output lines are generated by a scale-dependent variable averaging (YACL + 2) input lines. In this way a vertical FIR filter can be created for anti-aliasing, with up to 65 taps (max.).

YSCI defines the output line qualifier pattern and YACL defines the sequence length for the line averaging. For accurate processing, the sequence has to fit into the qualifying pattern. In the event of mis-programming YACL unexpected line dropping occurs; where N_{OL} = number of output lines and N_{IL} = number of input lines. The I²C-bus bits YSCI (scaling increment), YACL (accumulation length; optimum: 1 line overlap) and YP (scaling start phase) have to be set according to the following equations (see Fig.15):

$$YACL = TRUNC \times \left(\frac{N_{IL}}{N_{OL} - 1} \right);$$

accumulation sequence length: i.e. the number of lines per sequence that are not part of overlay region of neighbouring sequences (optimum 1 line overlapped).

$$YSCI = INT \left[1024 \times \left(\frac{1 - N_{OL}}{N_{IL}} \right) \right]$$; scaling increment.

$$YP = INT \left(\frac{YSCI}{16} \right)$$; scaling start phase (fix; modified in LPI mode only).

In order to obtain unity amplitude gain for all sequence lengths and to improve the vertical scaling performance, the accumulated lines can be weighted and the amplitude of the scaled output signal has to be renormalized. In the given example (see Fig.15) using the optimum weighting, the gain of a sequence results in 1 + 2 + 2 + 1 = 6. Renormalization (factor 1/6) can be achieved;

By gain reduction using BCS control (brightness, contrast and saturation) down to 4/6 and a selecting factor of 1/4 for DCGY2 to DCGY0 (see Section 8.3), which may result in a loss of signal quantization, or

By gain emphasizing using BCS control up to 8/6 and selecting a factor of 1/8 for DGY2 to DCGY0 which may result in a loss of signal detail, due to limiting in the BCS control.

Normally the weighting would be 2 + 2 + 2 + 2. In this situation the gain can be renormalized with DCGY2 to DCGY0 = 010 (factor 1/8).

Table 2 gives examples for I²C-bus register settings, depending on a given scale ratio.

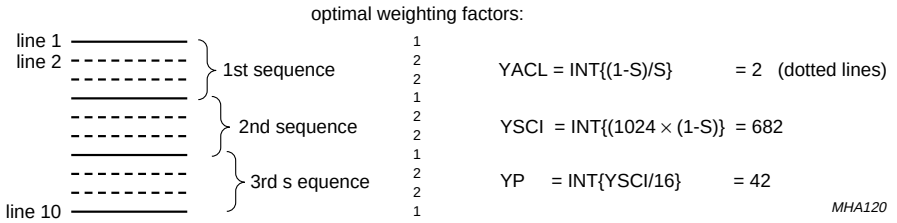


Fig.15 Example of vertical accumulation.

Table 2 Vertical scaling and normalization

VERTICAL SCALE RATIO (YSCI ≥)	YACL	COEFFICIENT SEQUENCE (example)	CYA (HEX)	CYB (HEX)	WEIGHT SUM	DCGY	BCS (CONT/SAT) = x/y × 64
1 to $\frac{1}{2}$ (0)	0	1-1	01	00	2	0	1
$\frac{1}{2}$ to $\frac{1}{3}$ (512)	1	1-1-1	03	00	3	0	$\frac{2}{3}$
		1-2-1	01	02	4	1	1
$\frac{1}{3}$ to $\frac{1}{4}$ (683)	2	1-1-1-1	03	00	4	1	1
$\frac{1}{4}$ to $\frac{1}{5}$ (768)	3	1-1-1-1-1	07	00	5	1	$\frac{4}{5}$
		1-2-2-2-1	01	06	8	2	1
$\frac{1}{5}$ to $\frac{1}{6}$ (820)	4	111 111	07	00	6	1	$\frac{4}{6}$
		121 121	05	02	8	2	1
		112 211	03	04	8	2	1
$\frac{1}{6}$ to $\frac{1}{7}$ (854)	5	111 1 111	0F	00	7	2	$\frac{8}{7}$
		111 2 111	07	08	8	2	1
$\frac{1}{7}$ to $\frac{1}{8}$ (878)	6	1111 1111	0F	00	8	2	1
$\frac{1}{8}$ to $\frac{1}{9}$ (896)	7	1111 1 1111	1F	00	9	2	$\frac{8}{9}$
		1222 2 2221	01	1E	16	3	1
$\frac{1}{9}$ to $\frac{1}{10}$ (911)	8	1111 1 1 1111	1F	00	10	3	$\frac{8}{10}$
		2121 2 2 1212	09	15	16	3	1
		1122 2 2 2211	03	1C	16	3	1
$\frac{1}{10}$ to $\frac{1}{11}$ (922)	9	1111 1 1 1 1111	3F	00	11	2	$\frac{8}{11}$
		1212 1 2 1 2121	15	2A	16	3	1
		1112 2 2 2 2111	07	38	16	3	1
$\frac{1}{11}$ to $\frac{1}{12}$ (931)	10	1111 11 11 1111	3F	00	12	2	$\frac{8}{12}$
		1211 21 12 1121	2D	12	16	3	1
		1111 22 22 1111	0F	30	16	3	1

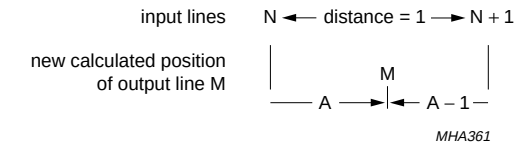
VERTICAL SCALE RATIO (YSCI ≥)	YACL	COEFFICIENT SEQUENCE (example)	CYA (HEX)	CYB (HEX)	WEIGHT SUM	DCGY	BCS (CONT/SAT) = x/y × 64
$\frac{1}{12}$ to $\frac{1}{13}$ (939)	11	1111 11 1 11 1111	7F	00	13	2	$\frac{8}{13}$
		1111 21 2 12 1111	2F	50	16	3	1
		1121 11 2 11 1211	3B	44	16	3	1
$\frac{1}{13}$ to $\frac{1}{14}$ (946)	12	1111 111 111 1111	7F	00	14	2	$\frac{8}{14}$
		1111 211 112 1111	6F	10	16	3	1
		1111 112 211 1111	3F	40	16	3	1
$\frac{1}{14}$ to $\frac{1}{15}$ (951)	13	1111 111 1 111 1111	FF	00	15	2	$\frac{8}{15}$
		1111 111 2 111 1111	7F	80	16	3	1
$\frac{1}{15}$ to $\frac{1}{16}$ (956)	14	1111 1111 1111 1111	FF	00	16	3	1
$\frac{1}{16}$ to $\frac{1}{17}$ (960)	15	1111 1111 1 1111 1111	FF	00	17	3	$\frac{16}{17}$
		2122 2222 2 2222 2212	02	FD	32	4	1
$\frac{1}{17}$ to $\frac{1}{18}$ (964)	16	1111 1111 1 1 1111 1111	FF	00	18	3	$\frac{16}{18}$
		2212 2212 2 2 2122 2122	44	BB	32	4	1
		1222 2222 1 1 2222 2221	01	FE	32	4	1
....	....	....	....	....	....	....	....
$\frac{1}{23}$ to $\frac{1}{24}$ (980)	22	1111 2222 1111 1111 2222 1111	0F	F0	32	4	1
		1121 1212 1121 1211 2121 1211	AD	52	32	4	1

7.4.2.2 LPI mode (scaling factor range 1 to $\frac{1}{2}$; IC-bus bit YACM = 0)

To preserve the signal quality for slight vertical downscales (scaling factors 1 to $\frac{1}{2}$) linear phase interpolation between consecutive lines is implemented to generate geometrically correct vertical output lines.Therefore, the new geometric position between lines N and N + 1 can be calculated.

A new output line is calculated by weighting the samples ‘p’ (pixel) of lines N and N + 1 with the normalized distance to the new calculated position (see Fig.16);

When N_{OL} = number of output lines and N_{IL} = number of input lines the I^2C-bus bits YSCI (scaling increment) and YP (scaling start phase) have to be set according to the following equations;



$$p(M) = A \times p(N+1) + (1-A) \times p(N)$$

where A = 0 to 63/64

Fig.16 New output line calculation.

$$YSCI = INT\left[1024 \times \left(\frac{N_{IL}}{N_{OL}} - 1\right)\right]$$; scaling increment

$$YP = INT\left(\frac{YSCI}{16}\right)$$; scaling start phase

(recommended value).

The vertical start phase offset is defined by $^{YP}/_{64}$ (YP = 0 to 64):

YP = 0: offset = 0 geometrical position of 1st line out = 1st line in.

YP = 64: offset = $^{64}/_{64}$ = 1 geometrical position of 1st line out = 2nd line in.

Finally 3 special modes must be emphasized:

1. By-pass (YSCI = 0, YP = 64) each line out is equivalent to corresponding line in.
2. Low-pass (YSCI = 0, YP < 64) e.g. YP = 32: average value of 2 lines ($1 + z^{-H}$ filter).
3. For processing of interlaced input signals the LPI mode **must** be used (the ACCU mode would cause 'line pairing' problems). The scaling start phase for odd and even field have to be set to:

   $$YP_{even} = YP_{odd} + \frac{YSCI}{32};$$

   where line 1 = odd.

In modes 1 and 2 the first input line is fed to the output (without processing) so that the number of output lines equals the number of input lines.

7.4.2.3 Flip option (FLIP = 1)

For both vertical scaling modes there is a flip option (mirroring) available for input lines with a maximum of 384 pixels. In the event that full screen pictures (e.g. 768×576) are to be flipped, they first have to be scaled down to 384 pixels per line in the horizontal prescaling unit. After vertical processing (flipping) they can be rezoomed to the original 768 pixels per line in the following VPD. It should be noted that when using the flip option, the last input line can not be displayed at the output.

7.4.3 HORIZONTAL VARIABLE PHASE SCALING

In the phase-correct horizontal variable phase scaling the pixels are calculated for the geometrical correct, orthogonal output pattern, down to $^1/_4$ of the prescaled pattern. In addition, a horizontal zooming feature is supported. The maximum zooming factor is at least 2, thus being even more dependent on input pattern and prescaling settings.

The phase scaling consists of a filter and arithmetic structure with 10 taps for the luminance and 4 taps for the chrominance processing. It is able to generate a phase-correct new pixel value, with virtually no phase or amplitude artefacts.

The new samples are calculated with a phase accuracy of $^1/_{64}$ of the pixel distance.

When using this circuit the up and down scaling is controlled by the I²C-bus parameters XSCI and XP. Because the variable phase scaling is restricted to downscale $>^1/_4$ of the fine scalers input pixel count, XSCI is also a function of the prescaling parameter XPSC.

As N_{IP} = number of input pixels per line (at SAA7140A input) and N_{OP} = number of desired output pixels/line, XSCI is defined by the following equation:

$$XSCI = INT\left[\frac{N_{IP}}{N_{OP}} \times \frac{1024}{(XPSC + 1)}\right]$$

The maximum value of XSCI = 4095. Zooming is performed for XSCI values less than 1024. The number of disqualified clock cycles between consecutive pixel qualifiers (at the phase scalers input) defines the maximum possible zoom factor. This means that zooming may also be a function of XPSC. It should be noted that implementation is dependent on a zooming factor greater than 2. Some artefacts may occur at the end of the zoomed line.

Internal rounding effects, may result in a deviation of ±1 output pixels compared to the expected result. In this situation, the I²C-bus parameter XP can be used to shift the starting phase of the phase calculation and thereby force an additional cycle to be disqualified.

In addition, when XP ≥ 128 it will force the internal phase calculation to fixed values, especially when XP = 128 it will force the phase scaler into bypass.

The scaled output data is fed back to the data formatter/reformatter unit and may be used as output signals from the bidirectional expansion port (if the mode is selected).

7.5 Colour Space Matrix (CSM), dither and gamma correction

The scaled YUV output data can be converted after Interpolation into RGB data in accordance with CCIR 601 recommendations.

The matrix equations considering the digital quantization are as follows;

R = Y + 1.375 V

G = Y – 0.703125 V – 0.34375 U

B = Y + 1.734375 U

For error diffusion a dither algorithm of the 5-bit truncation error RGB (5, 5, 5) is implemented.

An anti-gamma characteristic (γ = 1.4) is implemented at the matrix output to provide anti-gamma correction of the RGB data. The curve can be used (bit RTB = 0) to compensate gamma correction for linear data representation of the RGB output data.

The chroma signal keyer generates an alpha signal to achieve an RGB (5, 5, 5) + α output signal. Therefore, the processed UV data amplitudes are compared with thresholds set via the I^{2}C-bus. A logic 1 signal is generated if the amplitude is within the specified amplitude range, if the amplitude is outside the specified range a logic 0 is generated. Keying can be switched off by setting the lower limit higher than the upper limit.

For 16-bit YUV data formats or monochrome modes the CSM block is bypassed.

7.6 Output formatter and output FIFO register

In order to support various scaling applications, the output data at the VRAM port can be delivered in different formats and different transfer modes. Besides the 16-bit YUV format (see Section 7.1.1) the VRAM port also supports the data formats 24-bit RGB, 2 $\times$ 15-bit RGB + α or 8-bit grey scale.

Should the synchronous data transfer mode (transparent mode) be selected, the VRAM port will provide VCLK clock (clock rate of LLC) and PXQ (polarity via programming) on extra pins for use by the circuitry receiving the VRAM port data stream.

To ease frame buffer applications, an asynchronous transfer (burst or FIFO mode) can be selected. In this mode the VRAM ports VCLK has to be provided from an external source, with a maximum clock rate of 32 MHz. Only valid data is collected and transported.

7.6.1 Data formats and reference signals of the VRAM port

7.6.1.1 16-bit YUV (see Section 7.1.1)

The ordering of YUV bits and bytes at the VRAM port is identical to that of the SAA7196.

7.6.1.2 24-bit RGB:

The resampled YUV samples are converted into RGB (8 bits each). All three components have the same sample rate as luminance Y. Anti-gamma correction is available (programming). The alpha bit is generated as the chroma key in the UV domain.

Two RGB representations (code meanings) are supported:

1. The CCIR 601 orientated RGB representation defines code 16 for black and code 235 for full saturation.
2. The graphics display orientated RGB representation codes black with 00H and white with FFH.
   This representation can be achieved by corresponding programming of brightness (equals offset), contrast and saturation (equals gain) in the YUV domain.
   This format is used in the transparent mode and in the FIFO mode (one pixel at a time).

7.6.1.3 15-bit RGB (5, 5, 5) + α in 2 bytes

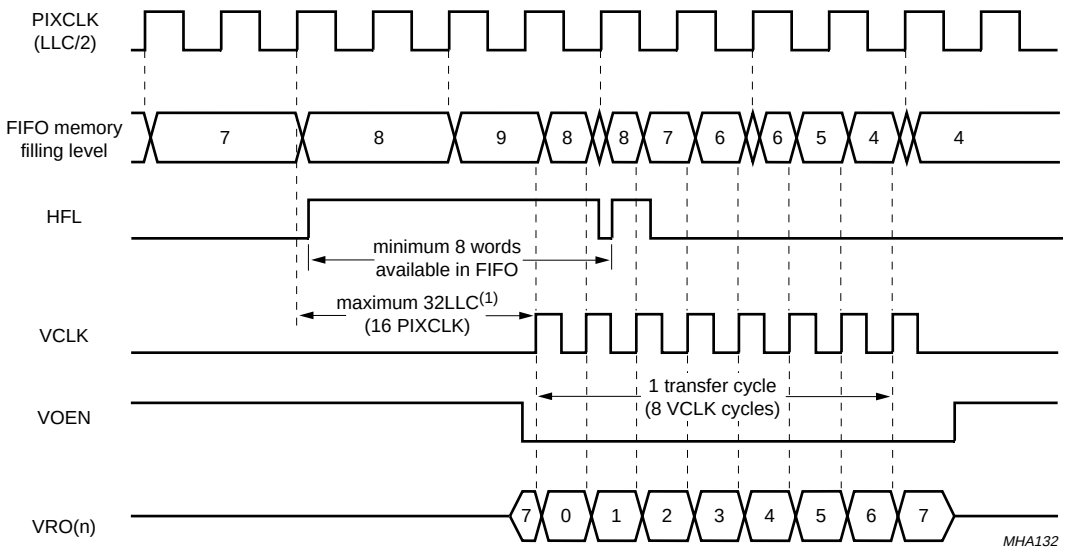
The resampled YUV samples are converted into 24-bit RGB. The following truncation to 5 bits is optionally (programming) performed with dithering effect (error diffusion). There are two representations (code meanings) supported; CCIR and graphics display orientated (see Section 7.6.1.2). The alpha bit is generated as chroma key in the YUV domain. This format is used in the transparent mode and in the FIFO mode (one pixel at a time, or two pixels at a time). The ordering of RGB bits and bytes at the VRAM port is identical to that of the SAA7196.

7.6.1.4 8-bit grey scale

This is simply a Y = luminance signal which can be selected to be coded as binary, or all bits inverted. This format is used in the transparent mode and in the FIFO mode (1, 2 or 4 pixels at a time).

The horizontal sync output HGTV marks (source independent) the range of the active video at the VRAM port.

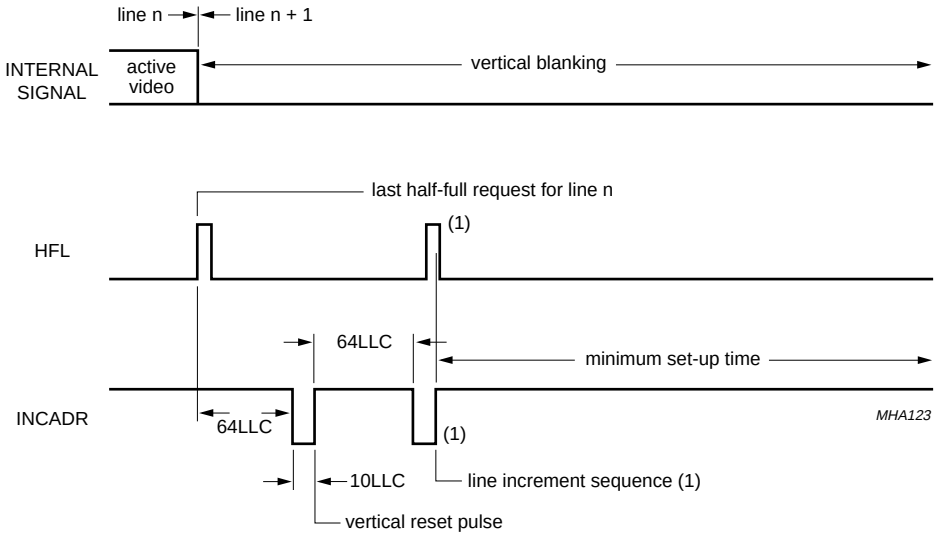
The vertical sync output VSYV (I^{2}C-bus controlled polarity) carries the vertical sync information for the VRAM port output data (positive or negative pulse with a length of 4 lines). At the falling or rising edge of VSYV the FLDV output is stable.



If VCLK cycles occur at VOEN = HIGH the FIFO register is unchanged but the outputs VRO31 to VRO0 remain in the 3-state position.

(1) Only valid for non-zoomed data.

Fig.17 Output port transfer to VRAM at 32-bit data format without scaling.



(1) Only available for interfaced processing at the beginning of an odd field.

Fig.18 Vertical reset timing of the VRAM port.

7.7 Data transfer modes

7.7.1 EXPANSION PORT MODES

The expansion port is controlled by I²C-bus subaddresses 02 (22H) and 03 (23H).

The expansion port can be configured in a very flexible way. Table 3 gives examples of the I²C-bus programming for several expansion port configurations. SAA7196 compatible modes are marked as ‘xx96’ in the MODE column. After reset the expansion port reference signal inputs are set to the ‘xxIO’ pins.

After reset the expansion port reference signal inputs are set to the ‘xxIO’ pins.

Pin FDIO can be used in the same way as the DIR pin of the SAA7196 if the I²C-bus bit FLDC is set to logic 1.

More information concerning the control signals can be found in Chapter 8. For correct application the user should first decide about some global interface properties before referring to this chapter such as:

- Does the application require separate input and output reference signal lines, if yes then I²C-bus bit SRIO = 0
- Does the application need hardware controlled I/O switching, if yes then I²C-bus bit FLDC = 1 and use of pin FDIO or
- Does software controlled I/O switching (register set controlled) the same job, if yes then I²C-bus bit FLDC = 0
- Which signal path defines the clock system
- Which signal path is the synchronization master
- Is dynamic field-wise switching required or is the source switching quite static, if static then do not be confused about odd or even; use SREGS and IREGS before referring to the I²C-bus section.

Table 3 Expansion port programming examples

MODE	FDIO	DAVE OUTPUT CONTROL [SUBADDRESS 02 (22H)]									SCALER INPUT CONTROL [SUBADDRESS 03 (23H)]					I/O
		YUV8 04 to 24H	FLDC	VIDC	VD1	VD0	HD1	HD0	PXQD	LLCD	SRIO	VSI	HSI	VIPSI	LLCS	
0	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	note 1
1	X	0	0	1	0	0	0	0	0	0	0	0	0	1	0	note 2
2	X	0	0	1	X	1	x	1	0	1	0	1	1	1	1	note 3
3	X	0	0	1	X	1	X	1	0	0	0	1	1	1	0	note 4
4	X	0	0	0	1	0	1	0	1	0	0	0	0	0	0	note 5
5	X	1	0	0	1	0	1	0	1	0	0	0	0	1	0	note 6
6	X	1	0	0	0	0	0	0	0	0	0	1	1	1	1	note 7
7	X	1	0	0	1	0	1	0	1	1	0	1	1	1	1	note 8
8	X	0	0	1	0	0	0	0	0	0	0	0	1	1	0	note 9
9	X	1	0	1	X	X	X	X	X	X	1	1	1	1	1	note 10
0 '96	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	note 11
1 '96	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	note 12
2 '96	1	0	1	1	x	X	X	X	X	X	1	1	1	1	1	note 13
3 '96	x	0	1	1	x	X	X	1	0	0	1	1	1	0	0	note 14
4 '96	1	0	1	1	0	0	X	X	X	0	1	0	1	1	0	note 15
5 '96	0	0	1	0	0	0	X	X	X	0	1	0	0	1	1	note 16
6 '96	1	0	1	0	0	0	X	X	X	0	1	0	0	1	1	note 17
																note 18

Notes

1. Scaler input from LLC, Y/UVIN, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, Y/UVIN, CREF, HREF and VS.
2. Scaler input from LLC, VIDH|L, PXQIN, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, HREF and VS.
3. Scaler input from LLCIN, VIDH|L, PXQIN, HIN and VIN; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLCIN, d.c., CREF, HIN and VIN.
4. Scaler input from LLC, VIDH|L, PXQIN, HIN and VIN; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, HIN and VIN.

5. Scaler input from LLC, Y|UVIN, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, YUVsc, Psc, Hsc and Vsc.
6. Scaler input from LLC, VIDL, PXQIN, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, YUVsc->VIDH, Psc, Hsc and Vsc.
7. Scaler input from LLCIN, VIDL, PXQIN, HIN and VIN; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, Y|UVIN->VIDH, C+HREF and VS.
8. Scaler input from LLCIN, VIDL PXQIN, HIN and VIN; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLCIN, YUVsc->VIDH, Psc, Hsc and Vsc.
9. Scaler input from LLC, VIDH|L PXQIN, HIN and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, HREF and VS.
10. Scaler input from LLCIO, VIDH, PXQIO, HIO and VIO; expansion port output clock, data, qualifier, horizontal and vertical reference derived from d.c., d.c., d.c., d.c. and d.c..
11. Scaler input from LLC, Y|UVIN, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, Y|UVIN, CREF, HREF and VS.
12. Scaler input from LLC, VIDH|L, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, HREF and VS.
13. Scaler input from LLCIO, VIDH|L, PXQIO, HIO and VIO; expansion port output clock, data, qualifier, horizontal and vertical reference derived from d.c., d.c., d.c., d.c. and d.c..
14. Scaler input from LLC, VIDH|L, CREF, HIO and VIO; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, d.c. and d.c.
15. Scaler input from LLC, VIDH/L, PXQIO, HIO and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., d.c., d.c., HREF and VS.
16. Scaler input from LLC, Y/UVIN, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, Y/UVIN, CREF, HREF and VS.
17. Scaler input from LLCIO, VIDH/L, PXQIO, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from d.c., d.c., d.c., HREF and VS.
18. Fill in user specific configuration.

7.8 VRAM port modes

7.8.1 Data burst transfer mode (FIFO Mode)

Data transfer on the VRAM port is asynchronous (TTR = 0). This mode can be used for all output formats. Four signals for communication with the external memory are provided:

1. HFL flag: the half-full flag of the FIFO output register is raised when the FIFO contains at least 8 data words (HFL = HIGH). By setting HFL to logic 1, the SAA7140A and SAA7140B requests a data burst transfer, via the external memory controller, that has to start a transfer cycle within the next 32LLC cycles for 32-bit long word modes (16LLC cycles for 16 and 24-bit modes). If there are pixels in the FIFO at the end of the line, which are not transferred, the circuit fills up the FIFO register with 'fill pixels' until it is half-full and sets the HFL flag to request a data burst transfer. After the transfer is completed, HFL is used in combination with INCADR to indicate the line increments.
2. The INCADR output signal is used in combination with HFL to control horizontal and vertical address generation for a memory controller. The pulse sequence depends on field formats (interlace/non-interlace or odd/even fields) and control bits OF1 and OF0 (subaddress 01). This means that:
   a) HFL = 1 at the rising edge of INCADR: the END OF LINE is reached; request for line address increment
   b) HFL = 0 at the rising edge of INCADR: the END OF FIELD/FRAME is reached; request for line and pixel address reset
3. VCLK input signal to clock the FIFO register output data VRO(n). New data is placed on the VRO(n) port with the rising edge of VCLK (see Fig.17).
4. The VOEN input enables output data VRO(n). The outputs are in 3-state mode at VOEN = HIGH. VOEN changes only when VCLK is LOW. If VCLK pulses are applied when VOEN is HIGH, the outputs remain inactive but the FIFO register accepts the pulses.

7.8.2 Continuous data transfer mode (transparent mode)

Data transfer on the VRAM port can be achieved synchronously (TTR = 1), controlled by output reference signals at separate pins (except the α-signal) and a continuous clock output signal (clock rate of LLC) on the VCLK pin.

The SAA7140A and SAA7140B delivers a continuously processed data stream. Consequently, the extended formats of the VRAM port output are selected (bit FS2 = 1; see Tables 6 and 7).

The output reference signals have to be used to buffer qualified preprocessed RGB or YUV video data. The YUV data is only valid in qualified time slots. Control output signals (see Tables 6 and 7) are:

- α = keying signal of the chroma keyer (not on extra pin but in lower byte of VRO output)
- FLDV = odd/even field bit in accordance with the internal field processing
- VSYV = vertical sync signal, active polarity is defined by VSYP bit
- HGTV = horizontal gate signal, logic 1 marks the horizontal direction from XO to (XO + XS) lines
- PXQV = pixel qualifier signal, active polarity is defined by QPP bit.

Interlaced processing (OF bits, subaddress 01): to support correctly interlaced data storage, the scaler delivers two INCADR/HFL sequences in each qualified line and an additional INCADR/HFL sequence after the vertical reset sequence at the beginning of an odd field. Consequently, the scaled lines are automatically stored in the right sequence.

INCADR timing: the distance from the last half-full request (HFL) to the INCADR pulse may be longer than 64LLC. The state of HFL is defined for minimum 2LLC cycles afterwards.

Monochrome format (see Tables 6 and 7); If TTR = 1 and FS2 = 1 then Ya = Yb.

7.8.3 I²C-bus controlled pseudo sleep mode

To reduce the power consumption of the SAA7140A and SAA7140B during phases, where no scaling operations are requested in the application, it is possible to switch the SAA7140A and SAA7140B into a pseudo sleep mode.

This mode can be activated, if the clock input LLCIN is not used or if the hardware is able to pull the LLCIN input or the LLCIO pin (in input mode) down to logic 0.

In applications, which do not use LLCIN, then LLCIN should be connected to ground.

LLC has to be provided continuously.

To activate the ‘Sleep Mode’ the scalers processing has to be switched to one of the inactive clock inputs of the expansion port. For example, If LLCIO is used as input and output in the application then:

LLCIN grounded => ‘Sleep Mode’ is active, if I²C-bus bits FLDC = 0, SRIO = 0 and LLCS = 1.

and If LLCIN is used as input and LLCIO is used as output:

LLCIN pulled down => ‘Sleep Mode’ is active, if I²C-bus bits FLDC = 0, SRIO = 0 and LLCS = 1.

LLCIO pulled down => ‘Sleep Mode’ is active, if I²C-bus bits FLDC = 0, SRIO = 1 and LLCS = 1.

To activate the scaler again, switch back to an active input clock, via SRIO and/or LLCS.

In ‘Sleep Mode’ the power consumption of the SAA7140A and SAA7140B is reduced to approximately 15% of its normal operational value.

Table 4 VRAM port output data formats (VRO31 to VRO16) at FS2 bit = 0 and VOF bit = 1 (can be set via I²C-bus), burst mode only, Pixel order = n, n + 1, n + 2, etc.

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB (5, 5, 5) + α 32-BIT WORDS(1)(2)			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 32-BIT WORDS(2)(3)			FS1 = 1; FS0 = 0 YUV 4 : 2 : 2 16-BIT WORDS(2)(3)			FS1 = 1; FS0 = 1 8-BIT MONOCHROME 32-BIT WORDS(4)		
	n	n + 2	n + 4	n	n + 2	n + 4	n	n + 1	n + 2	n n + 1	n + 4 n + 5	n + 8 n + 9
VRO31	α	α	α	Y_{e7}	Y_{e7}	Y_{e7}	Y_{e7}	Y_{o7}	Y_{e7}	Y_{a7}	Y_{a7}	Y_{a7}
VRO30	R4	R4	R4	Y_{e6}	Y_{e6}	Y_{e6}	Y_{e6}	Y_{o6}	Y_{e6}	Y_{a6}	Y_{a6}	Y_{a6}
VRO29	R3	R3	R3	Y_{e5}	Y_{e5}	Y_{e5}	Y_{e5}	Y_{o5}	Y_{e5}	Y_{a5}	Y_{a5}	Y_{a5}
VRO28	R2	R2	R2	Y_{e4}	Y_{e4}	Y_{e4}	Y_{e4}	Y_{o4}	Y_{e4}	Y_{a4}	Y_{a4}	Y_{a4}
VRO27	R1	R1	R1	Y_{e3}	Y_{e3}	Y_{e3}	Y_{e3}	Y_{o3}	Y_{e3}	Y_{a3}	Y_{a3}	Y_{a3}
VRO26	R0	R0	R0	Y_{e2}	Y_{e2}	Y_{e2}	Y_{e2}	Y_{o2}	Y_{e2}	Y_{a2}	Y_{a2}	Y_{a2}
VRO25	G4	G4	G4	Y_{e1}	Y_{e1}	Y_{e1}	Y_{e1}	Y_{o1}	Y_{e1}	Y_{a1}	Y_{a1}	Y_{a1}
VRO24	G3	G3	G3	Y_{e0}	Y_{e0}	Y_{e0}	Y_{e0}	Y_{o0}	Y_{e0}	Y_{a0}	Y_{a0}	Y_{a0}
VRO23	G2	G2	G2	U_{e7}	U_{e7}	U_{e7}	U_{e7}	V_{e7}	U_{e7}	Y_{b7}	Y_{b7}	Y_{b7}
VRO22	G1	G1	G1	U_{e6}	U_{e6}	U_{e6}	U_{e6}	V_{e6}	U_{e6}	Y_{b6}	Y_{b6}	Y_{b6}
VRO21	G0	G0	G0	U_{e5}	U_{e5}	U_{e5}	U_{e5}	V_{e5}	U_{e5}	Y_{b5}	Y_{b5}	Y_{b5}
VRO20	B4	B4	B4	U_{e4}	U_{e4}	U_{e4}	U_{e4}	V_{e4}	U_{e4}	Y_{b4}	Y_{b4}	Y_{b4}
VRO19	B3	B3	B3	U_{e3}	U_{e3}	U_{e3}	U_{e3}	V_{e3}	U_{e3}	Y_{b3}	Y_{b3}	Y_{b3}
VRO18	B2	B2	B2	U_{e2}	U_{e2}	U_{e2}	U_{e2}	V_{e2}	U_{e2}	Y_{b2}	Y_{b2}	Y_{b2}
VRO17	B1	B1	B1	U_{e1}	U_{e1}	U_{e1}	U_{e1}	V_{e1}	U_{e1}	Y_{b1}	Y_{b1}	Y_{b1}
VRO16	B0	B0	B0	U_{e0}	U_{e0}	U_{e0}	U_{e0}	V_{e0}	U_{e0}	Y_{b0}	Y_{b0}	Y_{b0}

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. e = even pixel numbers.
4. a and b = consecutive pixels.

Table 5 VRAM port output data formats (VRO15 to VRO0) at FS2 bit = 0 and VOF bit = 1 (can be set via I^2C-bus), burst mode only, Pixel order = n, 1n, 2n, etc.

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB (5, 5, 5) + α 32-BIT WORDS(1)(2)			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 32-BIT WORDS(2)(3)(4)			FS1 = 1; FS0 = 0 YUV 4 : 2 : 2 16-BIT WORDS(2)			FS1 = 1; FS0 = 1 8-BIT MONOCHROME 32-BIT WORDS(5)		
	n + 1	n + 3	n + 5	n + 1	n + 3	n + 5	OUTPUT NOT USED			n + 2 n + 3	n + 6 n + 7	n + 10 n + 11
VRO15	α	α	α	Y_{o7}	Y_{o7}	Y_{o7}	X	X	X	Y_{c7}	Y_{c7}	Y_{c7}
VRO14	R4	R4	R4	Y_{o6}	Y_{o6}	Y_{o6}	X	X	X	Y_{c6}	Y_{c6}	Y_{c6}
VRO13	R3	R3	R3	Y_{o5}	Y_{o5}	Y_{o5}	X	X	X	Y_{c5}	Y_{c5}	Y_{c5}
VRO12	R2	R2	R2	Y_{o4}	Y_{o4}	Y_{o4}	X	X	X	Y_{c4}	Y_{c4}	Y_{c4}
VRO11	R1	R1	R1	Y_{o3}	Y_{o3}	Y_{o3}	X	X	X	Y_{c3}	Y_{c3}	Y_{c3}
VRO10	R0	R0	R0	Y_{o2}	Y_{o2}	Y_{o2}	X	X	X	Y_{c2}	Y_{c2}	Y_{c2}
VRO9	G4	G4	G4	Y_{o1}	Y_{o1}	Y_{o1}	X	X	X	Y_{c1}	Y_{c1}	Y_{c1}
VRO8	G3	G3	G3	Y_{o0}	Y_{o0}	Y_{o0}	X	X	X	Y_{c0}	Y_{c0}	Y_{c0}
VRO7	G2	G2	G2	V_{e7}	V_{e7}	V_{e7}	X	X	X	Y_{d7}	Y_{d7}	Y_{d7}
VRO6	G1	G1	G1	V_{e6}	V_{e6}	V_{e6}	X	X	X	Y_{d6}	Y_{d6}	Y_{d6}
VRO5	G0	G0	G0	V_{e5}	V_{e5}	V_{e5}	X	X	X	Y_{d5}	Y_{d5}	Y_{d5}
VRO4	B4	B4	B4	V_{e4}	V_{e4}	V_{e4}	X	X	X	Y_{d4}	Y_{d4}	Y_{d4}
VRO3	B3	B3	B3	V_{e3}	V_{e3}	V_{e3}	X	X	X	Y_{d3}	Y_{d3}	Y_{d3}
VRO2	B2	B2	B2	V_{e2}	V_{e2}	V_{e2}	X	X	X	Y_{d2}	Y_{d2}	Y_{d2}
VRO1	B1	B1	B1	V_{e1}	V_{e1}	V_{e1}	X	X	X	Y_{d1}	Y_{d1}	Y_{d1}
VRO0	B0	B0	B0	V_{e0}	V_{e0}	V_{e0}	X	X	X	Y_{d0}	Y_{d0}	Y_{d0}

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. o = odd pixel numbers.
4. e = even pixel numbers.
5. c and d = consecutive pixels.

Table 6 VRAM port output data formats (VRO31 to VRO16) at FS2 bit = 1 and VOF bit = 1 (can be set via I^2C-bus), burst and transparent mode, Pixel order = n, n + 1, n + 2, etc.

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB (5, 5, 5) + α 16-BIT WORDS(1)(2)			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 16-BIT WORDS(2)(3)			FS1 = 1; FS0 = 0 RGB (8, 8, 8) 24-BIT WORDS(2)			FS1 = 1; FS0 = 1 8-BIT MONOCHROME 16-BIT WORDS(4)		
	n	n + 1	n + 2	n	n + 1	n + 2	n	n + 1	n + 2	n n + 1	n + 2 n + 3	n + 4 n + 5
VRO31	α	α	α	Y_{e7}	Y_{e7}	Y_{e7}	R7	R7	R7	Y_{a7}	Y_{a7}	Y_{a7}
VRO30	R4	R4	R4	Y_{e6}	Y_{e6}	Y_{e6}	R6	R6	R6	Y_{a6}	Y_{a6}	Y_{a6}
VRO29	R3	R3	R3	Y_{e5}	Y_{e5}	Y_{e5}	R5	R5	R5	Y_{a5}	Y_{a5}	Y_{a5}
VRO28	R2	R2	R2	Y_{e4}	Y_{e4}	Y_{e4}	R4	R4	R4	Y_{a4}	Y_{a4}	Y_{a4}
VRO27	R1	R1	R1	Y_{e3}	Y_{e3}	Y_{e3}	R3	R3	R3	Y_{a3}	Y_{a3}	Y_{a3}
VRO26	R0	R0	R0	Y_{e2}	Y_{e2}	Y_{e2}	R2	R2	R2	Y_{a2}	Y_{a2}	Y_{a2}
VRO25	G4	G4	G4	Y_{e1}	Y_{e1}	Y_{e1}	R1	R1	R1	Y_{a1}	Y_{a1}	Y_{a1}
VRO24	G3	G3	G3	Y_{e0}	Y_{e0}	Y_{e0}	R0	R0	R0	Y_{a0}	Y_{a0}	Y_{a0}
VRO23	G2	G2	G2	U_{e7}	U_{e7}	U_{e7}	G7	G7	G7	Y_{b7}	Y_{b7}	Y_{b7}
VRO22	G1	G1	G1	U_{e6}	U_{e6}	U_{e6}	G6	G6	G6	Y_{b6}	Y_{b6}	Y_{b6}
VRO21	G0	G0	G0	U_{e5}	U_{e5}	U_{e5}	G5	G5	G5	Y_{b5}	Y_{b5}	Y_{b5}
VRO20	B4	B4	B4	U_{e4}	U_{e4}	U_{e4}	G4	G4	G4	Y_{b4}	Y_{b4}	Y_{b4}
VRO19	B3	B3	B3	U_{e3}	U_{e3}	U_{e3}	G3	G3	G3	Y_{b3}	Y_{b3}	Y_{b3}
VRO18	B2	B2	B2	U_{e2}	U_{e2}	U_{e2}	G2	G2	G2	Y_{b2}	Y_{b2}	Y_{b2}
VRO17	B1	B1	B1	U_{e1}	U_{e1}	U_{e1}	G1	G1	G1	Y_{b1}	Y_{b1}	Y_{b1}
VRO16	B0	B0	B0	U_{e0}	U_{e0}	U_{e0}	G0	G0	G0	Y_{b0}	Y_{b0}	Y_{b0}

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. e = even pixel numbers.
4. a and b = consecutive pixels.

Table 7 VRAM port output data formats (VRO15 to VRO0) at FS2 bit = 1 and VOF bit = 1 (can be set via I²C-bus), burst and transparent mode, Pixel order = n, n + 1, n + 2, etc.

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB (5, 5, 5) + α 16-BIT WORDS(1)(2)			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 16-BIT WORDS(1)(2)			FS1 = 1; FS0 = 0 RGB (8, 8, 8) 24-BIT WORDS(1)(2)			FS1 = 1; FS0 = 1 8-BIT MONOCHROME 16-BIT WORDS(1)		
	n	n + 1	n + 2	n	n + 1	n + 2	n	n + 1	n + 2	n n + 1	n + 2 n + 3	n + 4 n + 5
VRO15	X	X	X	X	X	X	B7	B7	B7	X	X	X
VRO140	X	X	X	X	X	X	B6	B6	B6	X	X	X
VRO13	X	X	X	X	X	X	B5	B5	B5	X	X	X
VRO12	X	X	X	X	X	X	B4	B4	B4	X	X	X
VRO11	X	X	X	X	X	X	B3	B3	B3	X	X	X
VRO10	X	X	X	X	X	X	B2	B2	B2	X	X	X
VRO9	X	X	X	X	X	X	B1	B1	B1	X	X	X
VRO8	X	X	X	X	X	X	B0	B0	B0	X	X	X
VRO7	α	α	α	α	α	α	α	α	α	α	α	α
VRO6	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO5	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO4	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO3	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO2	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO1	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO0	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)

Notes

1. α = keying bit.
2. RGB = digital signals.

Table 8 Optional VRAM port output data formats (VRO31 to VRO16) at FS2 bit = 0 and VOF bit = 0 (can be set via I²C-bus), burst mode only; Pixel order = n, n + 1, n + 2, etc.; VMUX = 1 or 0

PIXEL OUTPUT BITS	FS1 = 0, FS0 = 0 RGB (5, 5, 5) + α 32-BIT LONG WORD(1)(2)(3)				FS1 = 0, FS0 = 1 YUV 4 : 2 : 2 32-BIT LONG WORD(2)(4)				FS1 = 1, FS0 = 1 8-BIT MONOCHROME 32-BIT LONG WORD(5)			
	n		n + 2		n		n + 2		n n + 1		n + 4 n + 5	
	1	0	1	0	1	0	1	0	1	0	1	0
VRO31	α	Z	α	Z	Y_{e7}	Z	Y_{e7}	Z	Y_{a7}	Z	Y_{a7}	Z
VRO30	R4	Z	R4	Z	Y_{e6}	Z	Y_{e6}	Z	Y_{a6}	Z	Y_{a6}	Z
VRO29	R3	Z	R3	Z	Y_{e5}	Z	Y_{e5}	Z	Y_{a5}	Z	Y_{a5}	Z
VRO28	R2	Z	R2	Z	Y_{e4}	Z	Y_{e4}	Z	Y_{a4}	Z	Y_{a4}	Z
VRO27	R1	Z	R1	Z	Y_{e3}	Z	Y_{e3}	Z	Y_{a3}	Z	Y_{a3}	Z
VRO26	R0	Z	R0	Z	Y_{e2}	Z	Y_{e2}	Z	Y_{a2}	Z	Y_{a2}	Z
VRO25	G4	Z	G4	Z	Y_{e1}	Z	Y_{e1}	Z	Y_{a1}	Z	Y_{a1}	Z
VRO24	G3	Z	G3	Z	Y_{e0}	Z	Y_{e0}	Z	Y_{a0}	Z	Y_{a0}	Z
VRO23	G2	Z	G2	Z	U_{e7}	Z	U_{e7}	Z	Y_{b7}	Z	Y_{b7}	Z
VRO22	G1	Z	G1	Z	U_{e6}	Z	U_{e6}	Z	Y_{b6}	Z	Y_{b6}	Z
VRO21	G0	Z	G0	Z	U_{e5}	Z	U_{e5}	Z	Y_{b5}	Z	Y_{b5}	Z
VRO20	B4	Z	B4	Z	U_{e4}	Z	U_{e4}	Z	Y_{b4}	Z	Y_{b4}	Z
VRO19	B3	Z	B3	Z	U_{e3}	Z	U_{e3}	Z	Y_{b3}	Z	Y_{b3}	Z
VRO18	B2	Z	B2	Z	U_{e2}	Z	U_{e2}	Z	Y_{b2}	Z	Y_{b2}	Z
VRO17	B1	Z	B1	Z	U_{e1}	Z	U_{e1}	Z	Y_{b1}	Z	Y_{b1}	Z
VRO16	B0	Z	B0	Z	U_{e0}	Z	U_{e0}	Z	Y_{b0}	Z	Y_{b0}	Z

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. Z = high ohmic (3-state).
4. e = even pixel numbers.
5. a and b = consecutive pixels.

Table 9 Optional VRAM port output data formats (VRO15 to VRO0) at FS2 bit = 0 and VOF bit = 0 (can be set via I²C-bus), burst mode only; Pixel order = n, n + 1, n + 2, etc.; VMUX = 1 or 0

PIXEL OUTPUT BITS	FS1 = 0, FS0 = 0 RGB (5, 5, 5) + α 32-BIT LONG WORD(1)(2)(3)				FS1 = 0, FS0 = 1 YUV 4 : 2 : 2 32-BIT LONG WORD(2)(3)(4)(5)				FS1 = 1, FS0 = 1 8-BIT MONOCHROME 32-BIT LONG WORD(3)(6)			
		n + 1		n + 3		n + 1		n + 3		n + 2 n + 3		n + 6 n + 7
	1	0	1	0	1	0	1	0	1	0	1	0
VRO15	Z	α	Z	α	Z	Y_{o7}	Z	Y_{o7}	Z	Y_{c7}	Z	Y_{c7}
VRO14	Z	R4	Z	R4	Z	Y_{o6}	Z	Y_{o6}	Z	Y_{c6}	Z	Y_{c6}
VRO13	Z	R3	Z	R3	Z	Y_{o5}	Z	Y_{o5}	Z	Y_{c5}	Z	Y_{c5}
VRO12	Z	R2	Z	R2	Z	Y_{o4}	Z	Y_{o4}	Z	Y_{c4}	Z	Y_{c4}
VRO11	Z	R1	Z	R1	Z	Y_{o3}	Z	Y_{o3}	Z	Y_{c3}	Z	Y_{c3}
VRO10	Z	R0	Z	R0	Z	Y_{o2}	Z	Y_{o2}	Z	Y_{c2}	Z	Y_{c2}
VRO9	Z	G4	Z	G4	Z	Y_{o1}	Z	Y_{o1}	Z	Y_{c1}	Z	Y_{c1}
VRO8	Z	G3	Z	G3	Z	Y_{o0}	Z	Y_{o0}	Z	Y_{c0}	Z	Y_{c0}
VRO7	Z	G2	Z	G2	Z	V_{e7}	Z	V_{e7}	Z	Y_{d7}	Z	Y_{d7}
VRO6	Z	G1	Z	G1	Z	V_{e6}	Z	V_{e6}	Z	Y_{d6}	Z	Y_{d6}
VRO5	Z	G0	Z	G0	Z	V_{e5}	Z	V_{e5}	Z	Y_{d5}	Z	Y_{d5}
VRO4	Z	B4	Z	B4	Z	V_{e4}	Z	V_{e4}	Z	Y_{d4}	Z	Y_{d4}
VRO3	Z	B3	Z	B3	Z	V_{e3}	Z	V_{e3}	Z	Y_{d3}	Z	Y_{d3}
VRO2	Z	B2	Z	B2	Z	V_{e2}	Z	V_{e2}	Z	Y_{d2}	Z	Y_{d2}
VRO1	Z	B1	Z	B1	Z	V_{e1}	Z	V_{e1}	Z	Y_{d1}	Z	Y_{d1}
VRO0	Z	B0	Z	B0	Z	V_{e0}	Z	V_{e0}	Z	Y_{d0}	Z	Y_{d0}

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. Z = high ohmic (3-state).
4. o = odd pixel numbers.
5. e = even pixel number.
6. c and d = consecutive pixels.

8 I²C-BUS PROTOCOL

8.1 I²C-bus format

Table 10 I²C-bus format

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA0	ACK	X	DATAn	ACK	P

Table 11 Description of I²C-bus format

CODE	DESCRIPTION
S	START condition
Slave address	0111 00X = IICSA = LOW or 0111 001X = IICSA = HIGH
ACK	acknowledge generated by the slave
Subaddress	subaddress byte (if more than 1 data byte is transmitted then an auto-increment of the subaddress is performed)
Data	data byte
P	STOP condition
X	read/write control bit: X = 0, order to write (the circuit is slave receiver) X = 1, order to read (the circuit is slave transmitter)

Table 12 I²C-bus status byte (X in address byte = 1; 71H at IICSA = LOW or 73H at IICSA = HIGH)

FUNCTION	DATA BITS							
	D7	D6	D5	D4	D3	D2	D1	D0
Status byte (subaddress 20H)	ID3	ID2	ID1	ID0	X	X	X	X

Table 13 Function of status bits ID3 to ID0 (software model of SAA7140A and SAA7140B compatible)

ID3	ID2	ID1	ID0	VERSION
0	0	0	0	V0 (first version)

Remark: With the exception of subaddress 20H (read only) all I²C-bus registers are read/write registers.

8.2 I²C-bus bitmap

Table 14 I²C-bus decoder control; subaddress and data bytes for writing (X in address byte = 0; 70H at IICSA = LOW or 72H at IICSA = HIGH); programming set A: subaddress = 02H to 1FH

FUNCTION SUBADDRESS		DATA BITS								
		D7	D6	D5	D4	D3	D2	D1	D0	DF(1)
Initial settings expansion/DMSD	00	FSEL	RSEN(4)	SREGS	IREGS	INVOE	REVFLD	FICO1	FICO0	
Initial settings VRAM	01	VPE	TTR(4)	VOF	QPP	OF1	OF0	LW1	LW0	
Expansion port output control	02	FLDC	VIDC	VD1	VD0	HD1	HD0	PXQD	LLCD	
Expansion I/O control; scaler source control	03	VSYP(4)	SRIO(4)	REHAW	REVAW	VSI	HSI	VIPSI	LLCS	
Expansion/VRAM format control	04	SHVS	YUV8	MCT	RTB	DIT	FS2	FS1	FS0	
Luminance brightness	05	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0	
Luminance contrast	06	X	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0	
Chroma saturation	07	X	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0	
Horizontal window start(2)	08	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Horizontal window length(2)	09	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
(continue)	0A	X	XO10	XO9	XO8	X	XS10	XS9	XS8	
Horizontal phase offset	0B	XP7	XP6	XP5	XP4	XP3	XP2	XP1	XP0	
Vertical window start(3)	0C	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
Vertical window length(3)	0D	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
(continue)	0E	X	YO10	YO9	YO8	X	YS10	YS9	YS8	
Vertical phase offset	0F	X	YP6(4)	YP5	YP4	YP3	YP2	YP1	YP0	
Horizontal prescaling	10	X	XACM(4)	XPSC5	XPSC4	XPSC3	XPSC2	XPSC1	XPSC0	
Horizontal weighting control (select Y)	11	CXY7	CXY6	CXY5	CXY4	CXY3	CXY2	CXY1	CXY0	
Horizontal weighting control (select UV)	12	CXUV7	CXUV6	CXUV5	CXUV4	CXUV3	CXUV2	CXUV1	CXUV0	
Prefilter YUV	13	PFUV3	PFUV2	PFUV1	PFUV0	PFY3	PFY2	PFY1	PFY0	
Vertical interpolation control	14	FLIP	YACM	YACL5	YACL4	YACL3	YACL2	YACL1	YACL0	
Vertical weighting control 1	15	CYA7	CYA6	CYA5	CYA4	CYA3	CYA2	CYA1	CYA0	
Vertical weighting control 2	16	CYB7	CYB6	CYB5	CYB4	CYB3	CYB2	CYB1	CYB0	
DC gain normalization	17	X	DCGX2	DCGX1	DCGX0	X	DCGY2	DCGY1	DCGY0	
Horizontal scaling increment	18	XSCI7	XSCI6	XSCI5	XSCI4	XSCI3	XSCI2	XSCI1	XSCI0	
(continue)	19	X	X	X	X	XSCI11	XSCI10	XSCI9	XSCI8	
Vertical scaling increment	1A	YSCI7	YSCI6	YSCI5	YSCI4	YSCI3	YSCI2	YSCI1	YSCI0	
(continue)	1B	X	X	X	X	X	X	YSCI9	YSCI8	

FUNCTION SUBADDRESS		DATA BITS								
		D7	D6	D5	D4	D3	D2	D1	D0	DF[1]
Chroma keying upper limit for V	1C	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
Chroma keying lower limit for V	1D	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
Chroma keying upper limit for U	1E	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Chroma keying lower limit for U	1F	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	
Programming set B; subaddress = 22H to 3FH										
Read only register	20	ID3	ID2	ID1	ID0	X	X	X	X	
I/O port enable	21	PEN3[4]	PEN2[4]	PEN1[4]	PEN0[4]	PORT3	PORT2	PORT1	PORT0	
Expansion port output control	22	FLDC	VIDC	VD1	VD0	HD1	HD0	PXQD	LLCD	
Expansion I/O control; scaler source control	23	VSYP[4]	SRIO[4]	REHAW	REVAW	VSI	HSI	VIPSI	LLCS	
Expansion/VRAM format control	24	SHVS	YUV8	MCT	RTB	DIT	FS2	FS1	FS0	
Luminance brightness	25	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0	
Luminance contrast	26	X	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0	
Chroma saturation	27	X	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0	
Horizontal window start[5]	28	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Horizontal window length[5]	29	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
(continue)	2A	X	XO10	XO9	XO8	X	XS10	XS9	XS8	
Horizontal phase offset	2B	XP7	XP6	XP5	XP4	XP3	XP2	XP1	XP0	
Vertical window start[6]	2C	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
Vertical window length[6]	2D	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
(continue)	2E	X	YO10	YO9	YO8	X	YS10	YS9	YS8	
Vertical phase offset	2F	YPF	YP6[4]	YP5	YP4	YP3	YP2	YP1	YP0	
Horizontal prescaling	30	X	XACM[4]	XPSC5	XPSC4	XPSC3	XPSC2	XPSC1	XPSC0	
Horizontal weighting control (select Y)	31	CXY7	CXY6	CXY5	CXY4	CXY3	CXY2	CXY1	CXY0	
Horizontal weighting control (select UV)	32	CXUV7	CXUV6	CXUV5	CXUV4	CXUV3	CXUV2	CXUV1	CXUV0	
Prefilter YUV	33	PFUV3	PFUV2	PFUV1	PFUV0	PFY3	PFY2	PFY1	PFY0	
Vertical interpolation control	34	FLIP	YACM	YACL5	YACL4	YACL3	YACL2	YACL1	YACL0	
Vertical weighting control 1	35	CYA7	CYA6	CYA5	CYA4	CYA3	CYA2	CYA1	CYA0	
Vertical weighting control 2	36	CYB7	CYB6	CYB5	CYB4	CYB3	CYB2	CYB1	CYB0	
DC gain normalization	37	X	DCGX2	DCGX1	DCGX0	X	DCGY2	DCGY1	DCGY0	
Horizontal scaling increment	38	XSCI7	XSCI6	XSCI5	XSCI4	XSCI3	XSCI2	XSCI1	XSCI0	

FUNCTION SUBADDRESS		DATA BITS								
		D7	D6	D5	D4	D3	D2	D1	D0	DF[1]
(continue)	39	X	X	X	X	XSCI11	XSCI10	XSCI9	XSCI8	
Vertical scaling increment	3A	YSCI7	YSCI6	YSCI5	YSCI4	YSCI3	YSCI2	YSCI1	YSCI0	
(continue)	3B	X	X	X	X	X	X	YSCI9	YSCI8	
Chroma keying upper limit for V	3C	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
Chroma keying lower limit for V	3D	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
Chroma keying upper limit for U	3E	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Chroma keying lower limit for U	3F	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	

Notes

1. Default register contents to be filled in by hand.
2. Continued in 0A.
3. Continued in 0E.
4. Bits set to logic 1 after reset (all other bits set to logic 0 after reset).
5. Continued in 2A.
6. Continued in 2E.

8.3 Description of the I²C-bus bits

Tables 15 to 21 give the function of the register bits given in Table 14.

8.3.1 Initial settings for the expansion and DMSD port; subaddress 00H

Table 15 Field detection; data bits FICO1 to FICO0

FICO1	FICO0	DESCRIPTION
0	0	field sequence as detected from H and V sync signals
0	1	field sequence synchronized to H and V but noise limited
1	0	free running field sequence
1	1	reserved

Table 16 Reference edge selection for the V sync input of the field detection; data bit REVFLD

REVFLD	DESCRIPTION
0	rising edge is reference
1	falling edge is reference

Table 17 Polarity selection for the H sync input of the field detection (note 1); data bit INVOE

INVOE	DESCRIPTION
0	active LOW, e.g. for SAA71xx signals similar to HREF
1	active HIGH, e.g. for SAA71xx signals similar to HS

Note

1. INVOE may also be used for FDIO and FLDV output signal inversion

Table 18 Polarity of I²C-bus register set ID; data bit IREGS

IREGS	DESCRIPTION
0	register set ID as defined by SREGS
1	register set ID inverted

Table 19 Fix I²C-bus register set ID; data bit SREGS

SREGS	DESCRIPTION
0	register set ID toggles as detected and defined by FICO0 and FICO1
1	register set ID fixed to 1 (register set B selected)

Table 20 Enable of reference signals PXQIO, HIO, VIO, FDIO, LLCIO (expansion port) and PXQV, HGTV, VSYV, FLDV (VRAM port); data bit RSEN

RSEN	DESCRIPTION
0	reference signals enabled
1	reference signals disabled

Table 21 Field sync definition; data bit FSEL

FSEL	DESCRIPTION
0	V input for field detection to be handled as V sync signal
1	V input for field detection to be handled as frame sync signal

8.3.2 INITIAL SETTINGS FOR THE VRAM PORT; SUBADDRESS 01H

Table 22 First pixel position in VRO data for FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1 (YUV); data bits LW1 and LW0

LW1	LW0	BITS 31 to 24	BITS 23 to 16	BITS 15 to 8	BITS 7 to 0	REMARK
0	0	pixel 0	pixel 0	pixel 1	pixel 1	FS2 = 0; TTR = 0
0	1	pixel 0	pixel 0	pixel 1	pixel 1	
1	0	black	black	pixel 0	pixel 0	
1	1	black	black	pixel 0	pixel 0	

Table 23 First pixel position in VRO data for FS1 = 1; FS0 = 1 (monochrome)

LW1	LW0	BITS 31 to 24	BITS 23 to 16	BITS 15 to 8	BITS 7 to 0	REMARK
0	0	pixel 0	pixel 1	pixel 2	pixel 3	FS2 = 0; TTR = 0
0	1	black	pixel 0	pixel 1	pixel 2	
1	0	black	black	pixel 0	pixel 1	
1	1	black	black	black	pixel 0	
0	0	pixel 0	pixel 1	X	X	FS2 = 1; TTR = 0; LW only affects the grey scale format
0	1	black	pixel 0	X	X	
1	0	pixel 0	pixel 1	X	X	
1	1	black	pixel 0	X	X	

Table 24 Set output field mode; data bits OF1 to OF0

OF1	OF0	DESCRIPTION
0	0	both fields for interlaced storage
0	1	both fields for non-interlaced storage
1	0	odd fields only (even fields ignored) for non-interlaced storage
1	1	even fields only (odd fields ignored) for non-interlaced storage

Table 25 Pixel qualifier polarity flag; data bit QPP

QPP	DESCRIPTION
0	PXQV is active LOW (pin 41)
1	PXQV is active HIGH

Table 26 VRAM-port output format; data bit VOF

VOF	DESCRIPTION
0	enabling of 32 to 16-bit multiplexing via VMUX
1	disabling of 32 to 16-bit multiplexing via VMUX

Table 27 VRAM-port mode selection; data bit TTR

TTR	DESCRIPTION
0	FIFO mode (VRAM data burst transfer)
1	transparent mode

Table 28 VRAM-port outputs enable; data bit VPE

VPE	DESCRIPTION
0	HFL and INCADR inactive (HFL = LOW, INCADR = HIGH); VRO outputs in 3-state
1	HFL and INCADR enabled; VRO outputs dependent on VOEN

8.3.3 PORT I/O CONTROL; SUBADDRESS 21H

Table 29 Select direction of PORT3 to PORT0; data bits PEN3 to PEN0

PEN3 TO PEN0	DESCRIPTION
PENx = 0	PORTx set to output
PENx = 1	PORTx set to input

Table 30 Status of port I/O's, pins 32 (PORT3) to 35 (PORT0)

PORT3 to PORT0	DESCRIPTION
Write mode	set status of PORT3 to PORT0 registers (applied to pins 32 to 35 if PENx = 0)
Read mode	read status of PORT3 to PORT0; if PENx = 0 then status of PORTx register; if PENx = 1 then status of external driven data

8.3.4 REGISTER SET A (02H TO 1FH) AND B (22H TO 3FH)

Table 31 Source select for expansion port clock output LLCIO (note 1); data bit LLCD

LLCD	DESCRIPTION
0	source is clock from DMSD port
1	source is clock input from expansion port, as defined by SRIO

Note

1. The clock output on LLCIO may be disabled by I^2C-bus bits SRIO = 1 and LLCS = 1; see Table 37.

Table 32 Source select for expansion port pixel qualifier and data output at PXQIO and VIDH/VIDL[7 to 0] (note 1); data bit PXQD

PXQD	DESCRIPTION
0	sources are corresponding signals from DMSD port
1	sources are corresponding signals from scaler output

Note

1. The qualifier output on PXQIO may be disabled by I^2C-bus bits SRIO = 1 and VIPSI = 1; see Table 38.

Table 33 Source select for expansion port horizontal sync output HIO (note 1); data bits HD1 to HD0

HD1	HD0	DESCRIPTION
0	0	source is corresponding signal from DMSD port
0	1	source is HIN from expansion port (short-cut)
1	0	source is corresponding signal from scaler output
1	1	source is HIN from expansion port

Note

1. If SRIO and HSI = 1 then HIO output is disabled.

Table 34 Source select for expansion port vertical sync output VIO (note 1); data bits VD1 to VD0

VD1	VD0	DESCRIPTION
0	0	source is corresponding signal from DMSD port
0	1	source is VIN from expansion port (short-cut)
1	0	source is corresponding signal from scaler output
1	1	source is VIN from expansion port

Note

1. If SRIO and VSI = 1 then VIO output is disabled.

Table 35 I/O control for the expansion port data output VIDH7 to VIDH0 and VIDL7 to VIDL0 (dependent on YUV8 programming for FLDC = 0) (note 1); data bit VIDC

YUV8	VIDC	DESCRIPTION
0	0	VIDH = output, VIDL = output
0	1	VIDH = input, VIDL = input
1	0	VIDH = output, VIDL = input
1	1	VIDH = input, VIDL = output

Note

1. If FLDC and FDIO) = 1 the outputs VIDH/VIDL are disabled.

Table 36 FDIO I/O control and signal definition; data bit FLDC

FLDC	FDIO	DESCRIPTION
0	–	FDIO contains odd/even flag FLD and is switched to output
1	–	FDIO may be provided with a 7196 DIR like signal and is switched to input
–	0	LLCIO, PXQIO and VIDH/VIDL I/O definition as defined by the I^2C-bus parameters
–	1	selected outputs are forced to input mode and corresponding signals are used as scaler input

Table 37 Source select for scaler clock input; data bit LLCS (03H to 23H)

FLDC	FDIO	SRIO	LLCS	DESCRIPTION
X	X	X	0	source is LLC from DMSD port
X	X	0	1	source is LLCIN from expansion port
0	X	1	1	source is LLCIO input from expansion port, output is disabled
1	0	1	1	source is derived from LLCIO output; LLCD = 0 from LLC of decoder port, LLCD = 1 not allowed
1	1	1	1	source is LLCIO input from expansion port, output is disabled

Table 38 Source select for scaler data and pixel qualifier input; data bit VIPSI

FLDC	FDIO	SRIO	VIPSI	DESCRIPTION
0	X	X	0	source is data and CREF from DMSD port
0	X	–	1	source is data input VIDH/VIDL: when the pixel qualifier is PXQIN from expansion port FLDC = 0, FDIO = x, SRIO = 0 and VIPSI = 1; when the pixel qualifier is PXQIO from expansion port, output disabled FLDC = 0, FDIO = x, SRIO = 1 and VIPSI = 1;
1	0	–	X	source is derived from data output VIDH/VIDL, from decoder port for PXQD = 0, PXQD = 1 is not allowed: when the pixel qualifier is PXQIN from expansion port FLDC = 1, FDIO = 0, SRIO = 0 and VIPSI = x; when the pixel qualifier is CREF via the PXQIO output for PXQD = 0, PXQD = 1 is not allowed FLDC = 1, FDIO = 0, SRIO = 1 and VIPSI = x
1	1	–	X	source is data input VIDH/VIDL, output disabled, when the pixel qualifier is PXQIN from expansion port FLDC = 1, FDIO = 1, SRIO = 0 and VIPSI = x; when the pixel qualifier is PXQIO from expansion, port output disabled FLDC = 1, FDIO = 1, SRIO = 1 and VIPSI = x

Table 39 Source select for scaler horizontal sync input; data bit HSI

SRIO	HSI	DESCRIPTION
X	0	source is HREF from DMSD port
0	1	source is HIN from expansion port
1	1	source is HIO from expansion port, HIO output disabled

Table 40 Source select for scaler vertical sync input and field detection H/V; data bit VSI

SRIO	VSI	DESCRIPTION
X	0	source is VS from DMSD port; VS and HREF for field detection
0	1	source is VIN from expansion port; VIN and HIN for field detection
1	1	source is VIO from expansion port; VIO and HIO for field detection

Table 41 Reference edge selection for the V sync input of the acquisition window; data bit REVAW

REVAW	DESCRIPTION
0	rising edge is reference
1	falling edge is reference

Table 42 Reference edge selection for the H-sync input of the acquisition window; data bit REHAW

REHAW	DESCRIPTION
0	rising edge is reference
1	falling edge is reference

Table 43 Expansion-port clock and reference signal selection; data bit SRIO (see Tables 37 to 40)

SRIO	DESCRIPTION
0	clock and reference signals are taken from xxxIN pins
1	clock and reference signals are taken from xxxIO pin, xxxIN pins are ignored

Table 44 VSYV output signal polarity; data bit VSYP

VSYP	DESCRIPTION
0	VSYV contains 1 active V sync signals
1	VSYV contains 0 active V sync signals

Table 45 VRAM port output format select; data bits FS2 to FS0 (04H to 24H); see Tables 6 and 7

FS2	FS1	FS0	OUTPUT FORMAT
0	0	0	RGB (5, 5, 5) + α; 2 $\times$ 16-bit/pixel; 32-bit word length; RGB matrix on, VRAM output format
0	0	1	YUV 4 : 2 : 2; 2 $\times$ 16-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
0	1	0	YUV 4 : 2 : 2; 1 $\times$ 16-bit/pixel; 16-bit word length; RGB matrix off, optional output format
0	1	1	monochrome mode; 4 $\times$ 8-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
1	0	0	RGB (5, 5, 5) + α; 1 $\times$ 16-bit/pixel; 16-bit word length; RGB matrix on, VRAM output + transparent format
1	0	1	YUV 4 : 2 : 2 + α; 1 $\times$ 16-bit/pixel; 16-bit word length; RGB matrix off; VRAM output + transparent format
1	1	0	RGB (8, 8, 8) + α; 1 $\times$ 24-bit/pixel; 24-bit word length; RGB matrix on, VRAM output + transparent format
1	1	1	monochrome mode; 2 $\times$ 8-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format

Table 46 Dithering (noise shaping) control (for VRAM port only); data bit DIT

DIT	DESCRIPTION
0	dithering on
1	dithering off

Table 47 ROM table for anti-gamma correction (for VRAM port only); data bit RTB

RTB	DESCRIPTION
0	ROM table switched on
1	ROM table switched off

Table 48 Monochrome and two's complement output data select; data bit MCT

MCT	DESCRIPTION
0	inverse grey scale luminance (if grey scale is selected by FS bits) or straight binary U, V data output
1	non-inverse monochrome luminance (if grey scale is selected by FS bits) or two's complement U, V data output

Table 49 Expansion port data path configuration; data bit YUV8; see Tables 8 and 9

YUV8	DESCRIPTION
0	expansion port set to 16-bit YUV
1	expansion port set to 8-bit YUV (VIDL7 to VIDL0)

Table 50 Select field sequence, H and V; data bit SHVS

SHVS	DESCRIPTION
0	use separate H and V input signals
1	use decoded information from the CCIR 656 data stream (only for YUV8 = 1)

Table 51 Luminance brightness control; data bits BRIG7 to BRIG0 (05H to 25H)

D7	D6	D5	D4	D3	D2	D1	D0	GAIN
1	1	1	1	1	1	1	1	255 (bright)
...	...	...	...	...	...	...	...	....
1	0	0	0	0	0	0	0	128 (CCIR level)
...	...	...	...	...	...	...	...	....
0	0	0	0	0	0	0	0	0 (dark)

Table 52 Luminance contrast control; data bits CONT6 to CONT0 (06H to 26H)

D7	D6	D5	D4	D3	D2	D1	D0	GAIN
0	1	1	1	1	1	1	1	1.999 (maximum contrast)
...	...	...	...	...	...	...	...	....
0	1	0	0	0	0	0	0	1 (CCIR level)
...	...	...	...	...	...	...	...	....
0	0	0	0	0	0	0	0	0 (luminance off)

Table 53 Chrominance saturation control; data bits SATN6 to SATN0 (07H to 27H)

D7	D6	D5	D4	D3	D2	D1	D0	GAIN
0	1	1	1	1	1	1	1	1.999 (maximum contrast)
...	...	...	...	...	...	...	...	....
0	1	0	0	0	0	0	0	1 (CCIR level)
...	...	...	...	...	...	...	...	....
0	0	0	0	0	0	0	0	0 (colour off)

Table 54 X (horizontal) offset definition, counted in input pixel qualifiers; data bits XO10 to XO0

XO10 to XO0	DESCRIPTION
08H to 28H and 0AH to 2AH	Defines the start position of the X processing window

Table 55 X (horizontal) source size definition, counted in input pixel qualifiers; data bits XS10 to XS0

XS10 to XS0	DESCRIPTION
09H to 29H and 0AH to 2AH	defines the length of the X processing window

Table 56 Start phase for horizontal variable phase scaling (defined by XSCI11 to XSCI0); data bits XP6 to XP0

XP6 to XP0	DESCRIPTION
0BH to 2BH	$XP_{START} = XP/128 \times T_{PXQ}$ (T_{PXQ} = distance between 2 pixels)

Table 57 X phase value fixed; data bit XP7

XP7	DESCRIPTION
0	sample phase is calculated for every qualified sample
1	sample phase is fixed to the value set by XP6 to XP0

Table 58 Y (vertical) offset definition, counted in input horizontal sync events; YO10 to YO0

YO10 to YO0	DESCRIPTION
0CH to 2CH and 0EH to 2EH	defines the start position of the Y processing window

Table 59 Y (vertical) source size definition, counted in input horizontal sync events; YS10 to YS0

YS10 to YS0	DESCRIPTION
0DH to 2DH and 0EH to 2EH	defines the length of the Y processing window

Table 60 Start phase for vertical scaling (defined by YSCI9 to YSCI0); data bits YP6 to YP0

YP6 to YP0	DESCRIPTION
0FH to 2FH	$YP_{START} = YP/128 \times T_{LINE}$ (T_{LINE} = distance between 2 lines)

Table 61 Prescaling factor of the X prescaler; data bits XPSC5 to XPSC0

XPSC5 to XPSC0	DESCRIPTION
10H to 30H	defines accumulation sequence length and subsampling factor of the input data stream where N_{OP} (XPSC) = TRUNC [N_{IN} / (XPSC + 1)] N_{OP} = number of prescaler output pixel and N_{IN} = number of qualified scaler input pixel

Table 62 X (horizontal) prescaler accumulation mode of accumulating FIR; data bit XACM

XACM	DESCRIPTION
0	accumulating operates overlapping
1	non overlapping accumulation (must be set to bypass the prescaler)

Table 63 Coefficient select for X prescaler (luminance component Y); data bits CXY7 to CXY0

CXY7 to CXY0	DESCRIPTION
11H to 31H	for DC gain compensation of prescaler the accumulated pixels can be weighted by 1 or 2. CXYi defines a sequence of 8 bits, which control the coefficients; when CXYi = 0 pixel weighted by 1 and when CXYi = 1 pixel weighted by 2

Table 64 Coefficient select for X prescaler (colour difference signals UV); data bits CXUV7 to CXUV0

CXUV7 to CXUV0	DESCRIPTION
12H to 32H	for DC gain compensation of prescaler the accumulated pixels can be weighted by 1 or 2. CXUVi defines a sequence of 8 bits, which control the coefficients; when CXUVi = 0 pixel weighted by 1 and when CXUVi = 1 pixel weighted by 2

Table 65 Prefilter selection for luminance component Y (note 1); data bits PFY3 to PFY0 (13H to 33H)

PFY1	PFY0 ≥	H1(z)	H2(z)	H3(z)
0	0	bypass	bypass	bypass
0	1	active	bypass	bypass
1	0	active	bypass	active
1	1	active	active	active

Note

1. $H(z) = H1(z) \times H2(z) \times H3(z)$ with $H1$ and $H3 = 1 + z^{-1}$; $H2 = 1 + A \times z^{-1} + z^{-2}$ and A = 2, $^{15}/_{16}$, $^{7}/_{8}$, $^{3}/_{4}$ for PFY3 and PFY2 = 00, 01, 10, 11.

Table 66 Prefilter selection for colour difference signals UV (note 1); data bits PFUV3 to PFUV0

PFUV1	PFUV0 ≥	H1(z)	H2(z)	H3(z)
0	0	bypass	bypass	bypass
0	1	active	bypass	bypass
1	0	active	active	bypass
1	1	active	active	active

Note

1. $H(z) = H1(z) \times H2(z) \times H3(z)$ with $H1 = 1 + z^{-1}$; $H2 = 1 + A \times z^{-1} + z^{-2}$; $H3 = 1 + z^{-2}$ and A = 2, $^{15}/_{16}$, $^{7}/_{8}$, $^{3}/_{4}$ for PFUV3 and PFUV2 = 00, 01, 10, 11.

Table 67 Accumulation sequence length of the Y (vertical) processing; data bits YACL5 to YACL0

YACL5 to YACL0	DESCRIPTION
14H to 34H	defines vertical accumulation sequence length of input lines. If accumulation FIR filter mode is selected (YACM), YACL has to fit to the vertical scaling factor (defined by YSCI9 to YSCI0)

Table 68 Y (vertical) scaler accumulation (respectively calculation) mode of vertical arithmetic; data bit YACM

YACM	DESCRIPTION
0	arithmetic operates as a linear phase interpolator (LPI)
1	arithmetic operates as accumulating FIR filter in vertical direction

Table 69 Horizontal flip ‘mirroring’; maximum pixels after prescaling = 384; data bit FLIP

FLIP	DESCRIPTION
0	output lines correspond to input lines
1	output lines correspond flipped input lines (see Section 7.4.2)

Table 70 Coefficient select for Y (vertical) processing in accumulation mode (notes 1 and 2); data bits CYA7 to CYA0 and CYB7 to CYB0 (15H to 35H and 16H to 36H)

CYBi	CYAi	CYi	WEIGHTING FACTOR
0	0	0	0
0	1	1	1
1	0	2	2
1	1	3	4

Notes

1. For improvement of vertical filtering the accumulated lines can be weighted. Weighting factor = $2^{(2 \times CYBi + CYAi - 1)}$
2. The resulting factor as a function of a bit pattern CYAi, CYBi and the DC gain control DCGY, is given in Tables 71 and 72.

Table 71 DC gain control of vertical scaler (see Table 2) (notes 1, 2 and 3) ; data bits DCGY2 to DCGY0 (17H to 37H)

DCGY2	DCGY1	DCGY0	DCGY	GAIN FACTOR
0	0	0	0	2
0	0	1	1	4
...	....	....	....	....
...	....	....	....	....
1	1	1	7	256

Notes

1. Dependent on active coefficients and the sequence length, the amplitude gain has to be renormalized.
2. Gain factor = $2^{(DCGY + 1)}$.
3. The resulting factor is a function of CYi and DCGY; 0 for (CYAi = CYBi = 0) or (CYAi = CYBi = 1 and DCGY = 0) or (DGCY > 5). The weighting/gain factor is given in Table 72.

Table 72 Weighting factor as a function of gain factor

CYI	DCGY0	DCGY1	DCGY2	DCGY3	DCGY4	DCGY5	DCGY6	DCGY7
0	0	0	0	0	0	0	0	0
1	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	$\frac{1}{64}$	0	0
2	1	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	0	0
3	0	1	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	0	0

Table 73 DC gain control of horizontal prescaler (see Table 1; note 1); data bits DCGX2 to DCGX0

DCGX2	DCGX1	DCGX0	GAIN
0	0	0	$\times 1$
0	0	1	$\times \frac{1}{2}$
0	1	0	$\times \frac{1}{4}$
0	1	1	$\times \frac{1}{8}$
1	0	0	$\times \frac{1}{2}$
1	0	1	$\times \frac{1}{4}$
1	1	0	$\times \frac{1}{8}$
1	1	1	$\times \frac{1}{16}$

Note

1. Dependent on the number of active coefficients ‘2’ in the accumulation sequence and the sequence length, the output amplitude gain has to be renormalization via DCGX.

Table 74 X scaler increment for variable phase scaling in horizontal pixel phase arithmetic (note 1); data bits XSCI11 to XSCI0 (18H to 38H and 19H to 39H)

XSCI11 TO XSCI0	DESCRIPTION
18H to 38H and 19H to 39H	$XSCI = INT\left[\frac{N_{IP}}{N_{OP}} \times \frac{1024}{(XPSC + 1)}\right]$

Note

1. Where N_{IP} = number of qualified scaler input pixel and N_{OP} = number of output pixel.

Table 75 Y scaler increment for vertical down scaling; data bits YSCI9 to YSCI0 (1Ah to 3Ah and 1BH to 3BH)

YSCI9 TO YSCI0	DESCRIPTION
1AH to 3AH	$YSCI = INT\left[1024 \times \left(\frac{N_{IL}}{N_{OL}} - 1\right)\right]$; for YACM = 0 = LPI mode
1BH to 3BH	$YSCI = INT\left[1024 \times \left(1 - \frac{N_{OL}}{N_{IL}}\right)\right]$; for YACM = 1 = accumulation mode

Table 76 Set upper limit V for colour keying (8-bit; two’s complement); data bits VU7 to VU0 (1CH to 3CH)

VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	DESCRIPTION
1	0	0	0	0	0	0	0	as maximum negative value = –128 signal level
0	0	0	0	0	0	0	0	limit = 0
0	1	1	1	1	1	1	1	as maximum positive value = +127 signal level

Table 77 Set lower limit V for colour keying (8-bit; two’s complement); data bits VL7 to VL0 (1DH to 3DH)

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	DESCRIPTION
1	0	0	0	0	0	0	0	as maximum negative value = –128 signal level
0	0	0	0	0	0	0	0	limit = 0
0	1	1	1	1	1	1	1	as maximum positive value = +127 signal level

Table 78 Set upper limit U for colour keying (8-bit; two's complement); data bits UU7 to UU0 (1EH to 3EH)

UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	DESCRIPTION
1	0	0	0	0	0	0	0	as maximum negative value = –128 signal level
0	0	0	0	0	0	0	0	limit = 0
0	1	1	1	1	1	1	1	as maximum positive value = +127 signal level

Table 79 Set lower limit U for colour keying (8-bit; two's complement); data bits UL7 to UL0 (1FH to 3FH)

UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	DESCRIPTION
1	0	0	0	0	0	0	0	as maximum negative value = –128 signal level
0	0	0	0	0	0	0	0	limit = 0
0	1	1	1	1	1	1	1	as maximum positive value = +127 signal level

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DDD(bord)}$	digital supply voltage for I/O section	SAA7140A	–0.5	+6.5	V
$V_{DDD(core)}$	digital supply voltage for internal core	SAA7140A	–0.5	+6.0	V
V_{DDD}	digital supply voltage	SAA7140B	–0.5	+6.0	V
V_I	DC input voltage	SAA7140B	–0.5	V_{DDD} + 0.5	V
V_O	DC output voltage	SAA7140B	–0.5	V_{DDD} + 0.5	V
P_{tot}	total power dissipation	SAA7140A	–	750	mW
		SAA7140B	–	750	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
V_{esd}	electrostatic protection		2000[1]	–	V

Note

1. Pin 31 (SDA): 800 V.

10 HANDLING

Inputs and output are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	60	K/W

12 DC CHARACTERISTICS

$V_{DDD(bord)}$ = 4.5 to 5.5 V; $V_{DDD(core)}$ = 3.0 to 3.6 V; V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; SAA7140A						
$V_{DDD(bord)}$	digital supply voltage for I/O section		4.5	5.0	5.5	V
$V_{DDD(core)}$	digital supply voltage for internal core		3.0	3.3	3.6	V
$I_{DDD(bord)}$	digital supply current for I/O section	normal operation	–	30	–	mA
		sleep mode	–	10	–	mA
$I_{DDD(core)}$	digital supply current for internal core	normal operation	–	60	–	mA
		sleep mode	–	10	–	mA
$I_{DDD(tot)}$	total digital supply current		–	100	–	mA
Supplies; SAA7140B						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current	normal operation	–	90	–	mA
		sleep mode	–	10	–	mA
Data, clock and control inputs						
V_{IL}	LOW level input voltage	clocks	–0.5	–	0.6	V
V_{IH}	HIGH level input voltage	clocks	2.4	–	V_{DDD} + 0.5	V
V_{IL}	LOW level input voltage	other inputs; SAA7140A	–0.5	–	0.8	V
		other inputs; SAA7140B	–0.5	–	$0.2V_{DDD}$	V
V_{IH}	HIGH level input voltage	other inputs; SAA7140A	2.0	–	V_{DDD} + 0.5	V
		other inputs; SAA7140B	2.4	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	V_{IL} = 0 V	–	–	1	mA
C_I	input capacitance	data	–	–	8	pF
		clocks	–	–	8	pF
		3-state I/O; high-impedance state	–	–	8	pF
Data, clock and control outputs (note 1)						
V_{OL}	LOW level output voltage	all outputs; SAA7140A	0	–	0.6	V
		clocks; SAA7140B	0	–	0.4	V
V_{OH}	HIGH level output voltage	clocks; SAA7140A	2.6	–	V_{DDD}	V
		clocks; SAA7140B	$0.85V_{DDD}$	–	V_{DDD}	V
V_{OH}	HIGH level output voltage	other outputs; SAA7140A	2.4	–	V_{DDD}	V
		other outputs; SAA7140B	$0.85V_{DDD}$	–	V_{DDD}	V
V_{OL}	LOW level output voltage	other outputs; SAA7140B	0	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus, SDA and SCL (pins 31 and 32)						
V_{IL}	LOW level input voltage					
	SAA7140A		–0.5	–	+1.5	V
	SAA7140B		–0.5	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
$I_{31, 32}$	input current		–	–	±10	µA
I_{ACK}	output current on pin 31	acknowledge	3	–	–	mA
V_o	output voltage at acknowledge	I_{31} = 3 mA	–	–	0.4	V

Note

1. Levels measured with load circuit; 1.2 kΩ at 3 V (TTL load); C_L = 40 pF.

13 AC CHARACTERISTICS

$V_{DDD(bord)}$ = 4.5 to 5.5 V; $V_{DDD(core)}$ = 3.0 to 3.6 V; V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock input timing (LLC, LLCIN and LLCIO as input) (see Fig.20)						
t_{LLC}, t_{LLCIN}	cycle time		31	–	45	ns
δ	duty factor	t_{LLCH} or t_{LLC}	40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
VCLK input timing (for 'Burst Mode' only, TTR = 0); note 1 (see Fig.19)						
t_{VCLK}	VRAM port clock cycle time	note 2	30	–	200	ns
t_{pL}	VCLK LOW time	note 3	12	–	–	ns
t_{pH}	VCLK HIGH time	note 3	12	–	–	ns
t_r	rise time	0.6 V to $0.85V_{DDD}$	–	–	5	ns
t_f	fall time	$0.85V_{DDD}$ to 0.6 V	–	–	6	ns
Data and control input timing, related to the corresponding input clock; (see Fig.20)						
t_{SU}	set-up time		11	–	–	ns
t_{HD}	hold time		3	–	–	ns
Data and control input timing at the expansion port, related to LLCIO output						
t_{SU}	set-up time		15	–	–	ns
t_{HD}	hold time		0	–	–	ns
Clock output timing (LLCIO and VCLK output); note 4 (see Fig.20)						
C_L	output load capacitance		15	–	40	pF
t_{LLCIO}	cycle time		31	–	45	ns
δ	duty factor	t_{LLCIOH} or t_{LLCIO}	38	49	59	%
t_r	rise time	0.6 V to $0.85V_{DDD}$	–	–	5	ns
t_f	fall time	$0.85V_{DDD}$ to 0.6 V	–	–	6	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data and control output timing at the expansion port, related to LLCIO output; (see Fig.20)						
C_L	load capacitance		15	–	40	pF
t_{OHD}	output hold time	C_L = 7.5 pF	1.5	–	–	ns
		C_L = 15 pF	–	–	–	ns
t_{PD}	propagation delay from positive edge of LLCIO output	C_L = 40 pF	–	–	15	ns
VRO and reference signal output timing, related to VCLK output; (see Fig.19)						
C_L	output load capacitance	VRO outputs	15	–	40	pF
		other outputs	7.5	–	25	pF
t_{OHD}	VRO data hold time	C_L = 10 pF; note 5	0	–	–	ns
t_{OHL}	related to LCC scaler (INCADR, HFL)	C_L = 10 pF; notes 6 and 1	0	–	–	ns
t_{OHV}	related to VCLK (HFL)	C_L = 10 pF; note 6	0	–	–	ns
t_{OD}	VRO data delay time in burst mode (TTR = 0)	C_L = 40 pF; note 5	–	–	25	ns
	VRO data delay time in transparent mode (TTR = 1)	C_L = 40 pF; note 5	–	–	15	ns
t_{ODL}	related to LCC_{Scaler} (INCADR,HFL)	C_L = 25 pF; notes 6 and 7	–	–	60	ns
t_{ODV}	related to VCLK (HFL)	C_L = 25 pF; note 6	–	–	60	ns
t_D	VRO disable time to 3-state	C_L = 40 pF; note 7	–	–	40	ns
		C_L = 25 pF; note 8	–	–	24	ns
t_E	VRO enable time from 3-state	C_L = 40 pF; note 7	–	–	40	ns
		C_L = 25 pF; note 8	–	–	25	ns
$t_{HFL\ VOE}$	HFL rising edge to VRAM port enable	no zooming	–	–	810	ns
$t_{HFL\ VCLK}$	HFL rising edge to VCLK burst	no zooming	–	–	840	ns

Notes

1. LLC_{Scaler} may be LLC from DMSD port or LLCIN from expansion-port, dependent on scaler source clock selection via I^2C-bus bit LLCS.
2. Maximum T_{VCLK} = 200 ns for test mode only. The applicable maximum cycle time depends on data format, horizontal scaling and input data rate.
3. Measured at 1.5 V level; t_{pL} may be infinite.
4. $LLCIO_{out}$ timing also valid for VCLKout in transparent mode; (see Fig.20).
5. Timings of VRO refer to the rising edge of VCLK.
6. The timing of INCADR and the rising edge of HFL always refers to LLC_{Scaler}. During a VRAM transfer, the falling edge of HFL is generated by VCLK. During horizontal increment and vertical reset cycles, both edges of HFL always refer to LLC scaler.
7. Asynchronous signals. Its timing refers to the 1.5 V switching point of VOEN input signal (pin 53).
8. The timing refers to the 1.5 V switching point of VMUX signal (pin 46) in 32 to 16-bit multiplexing mode. Corresponding pairs of VRO outputs are together connected.

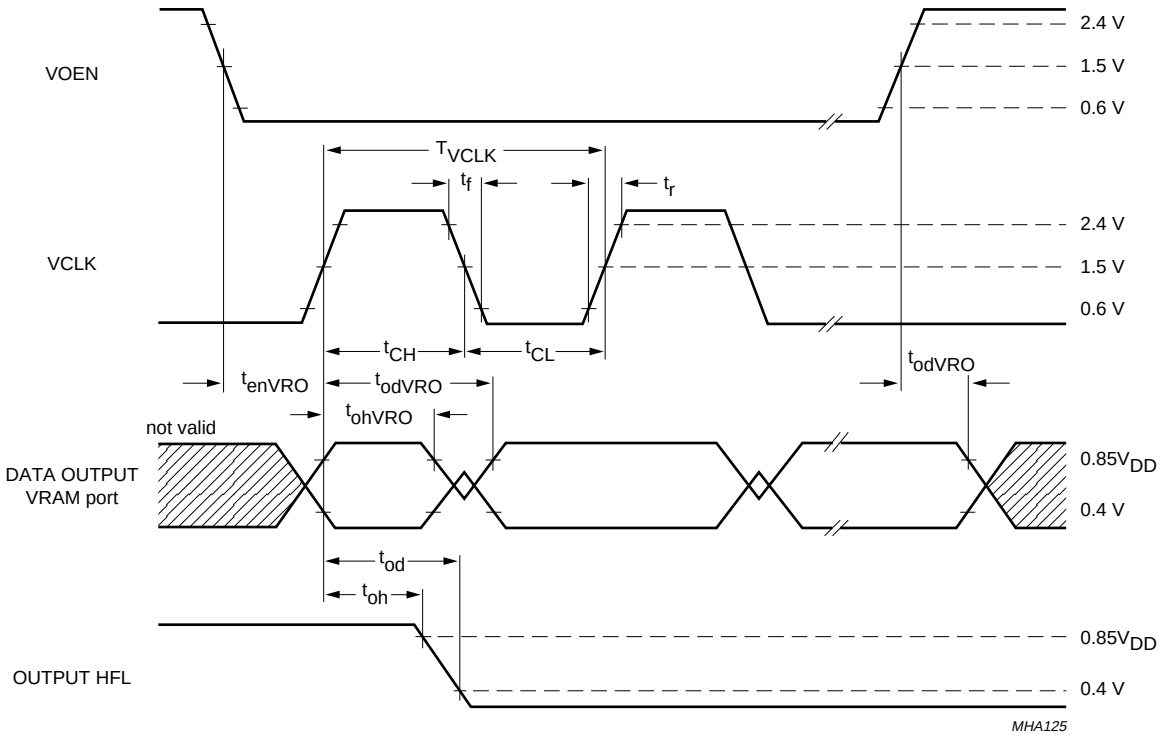


Fig.19 Data output timing (VRAM port).

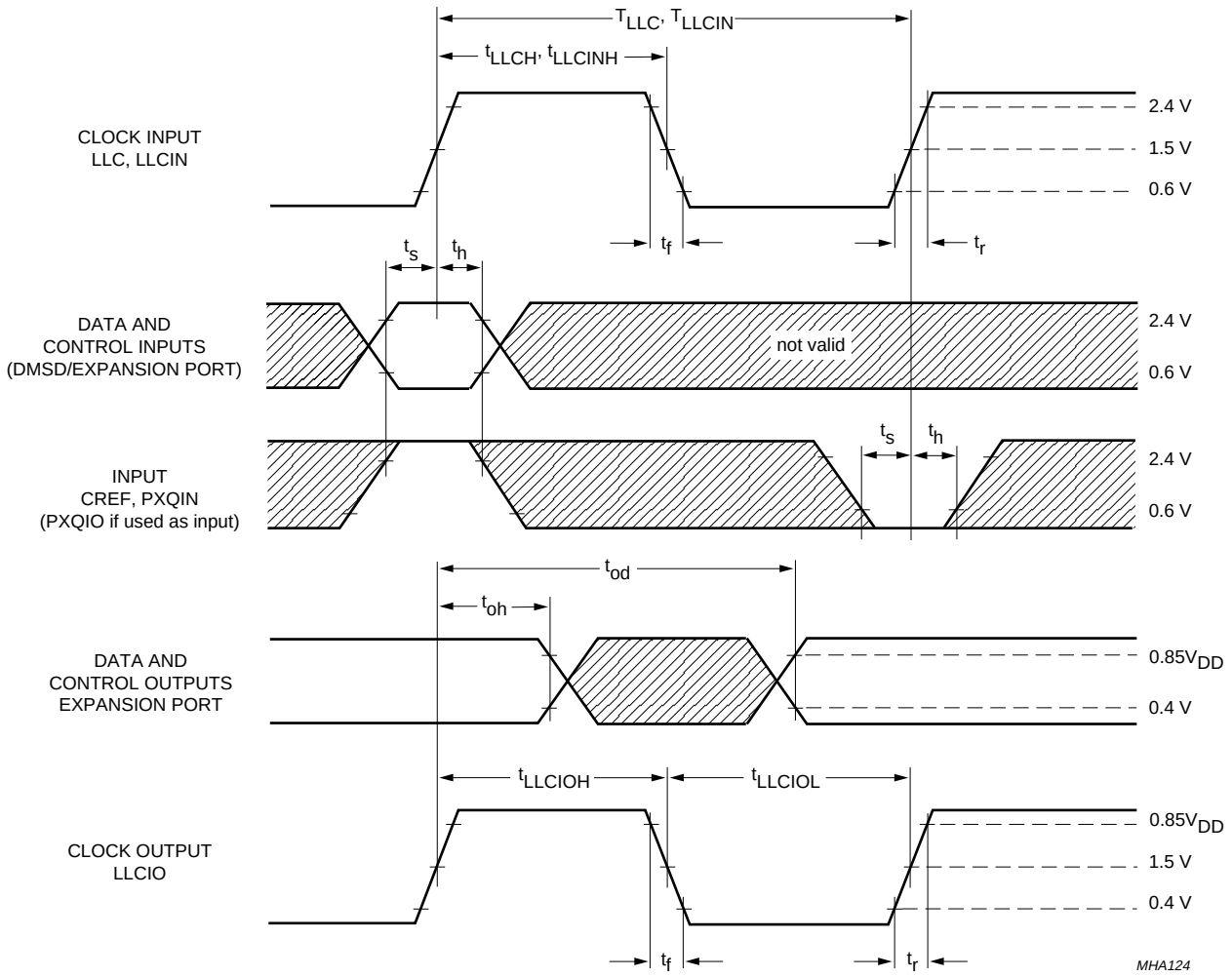
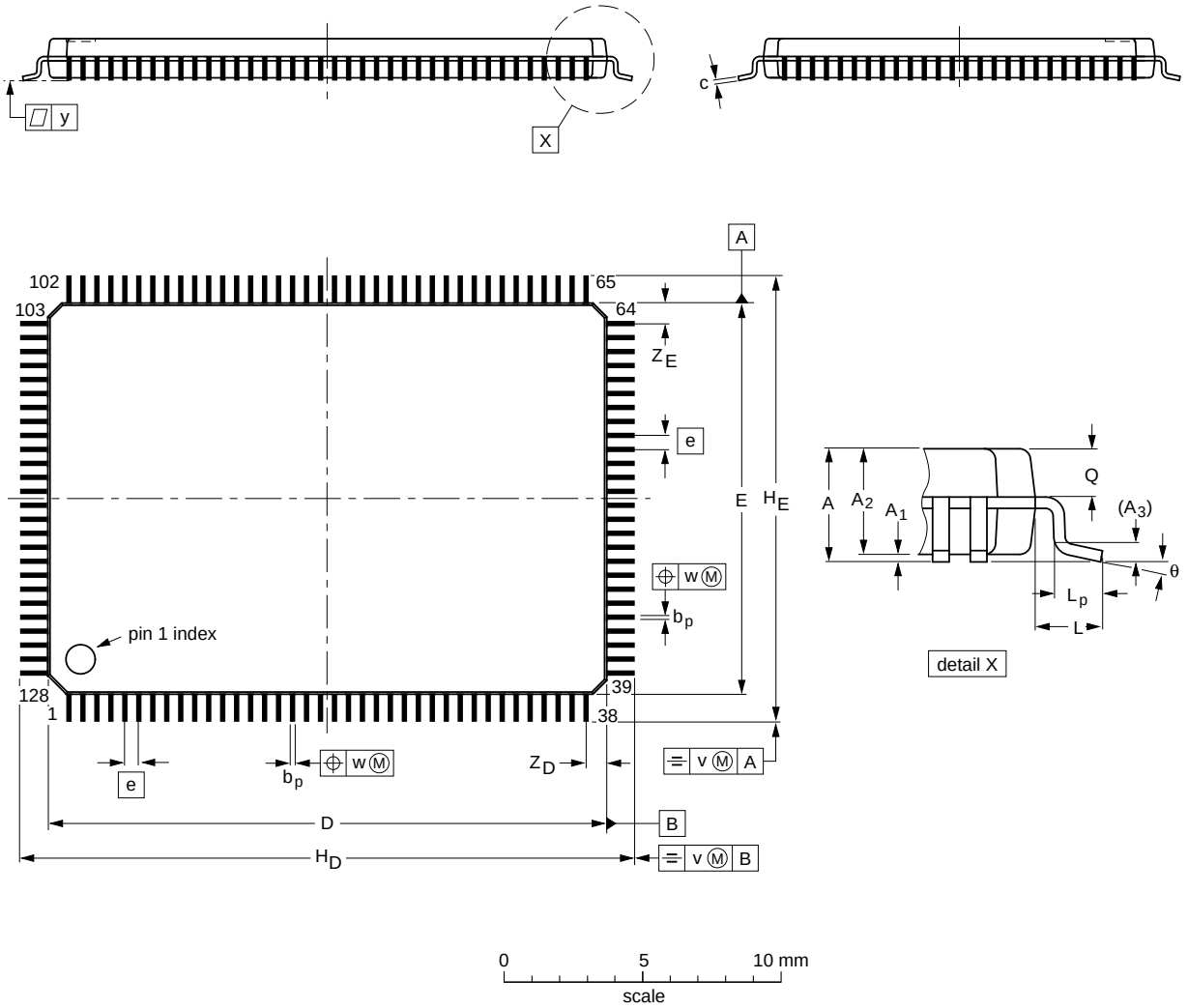


Fig.20 Data input/output timing (DMSD port and expansion port).

14 PACKAGE OUTLINE

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm **SOT425-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1.0	0.75 0.45	0.70 0.58	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT425-1						96-04-02

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

15.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP and SO packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

15.3 Wave soldering

15.3.1 QFP

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

15.3.2 SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

15.3.3 METHOD (QFP AND SO)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

18 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 926 5361, Fax. +7 095 564 8323

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 825 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 657021/1200/02/pp68 Date of release: 1996 Sep 04 Document order number: 9397 750 01068

Let's make things better.

Philips Semiconductors

PHILIPS